

FPGA: Accelerating FPGA Timing Closure for Complex FPGAs (8am-12pm)

Modern FPGA technology, with tremendous advances in both performance and capacity, is now a very viable solution for many high performance designs. Not only are FPGAs popularly used to minimize risks in both schedule and costs but also for their flexibility to accept design modifications during the product life cycle. Design methodologies must be tailored to confront the obstacles presented by these multi-million gate FPGA designs. These obstacles in addition to meeting design requirements include support for complex design flows, advanced language compatibility, and productivity enhancements.

Optimized for today's complex FPGA architectures, Mentor Graphics' Precision Synthesis utilizes sophisticated RTL and physical optimization algorithms to minimize the number of iterations to obtain the final complete design. Technology such as:

- Technology specific mapping and optimization
- Advanced design analysis
- Placement optimization
- Incremental design methodologies
- Placement reuse

are all included in a fully interactive environment that allows the designer to get products to market faster with the latest in FPGA technology.

This workshop will take the designer through:

- 1) Proper design constraint entry
- 2) Design optimization and analysis
- 3) Incremental changes
- 4) Placement re-use