

	Room 1	Room 2	Room 3	Room 4	Room 7	Room 8	
7:30 - 8:30	Registration / Continental Breakfast						
8:30 - 8:45	Opening Remarks						
	Board Station	PADS/Expedition	High-Speed	FPGA HDL Flow	General	IC - ASIC	
9:00 - 10:00	What's New in Board Station: Board Station XE	CES Package Type Clearance Rules	Effective Techniques for SERDES Channel Design	Accellera VHDL-2006	Introduction to VB	Extracting and Simulating Mixed Signal Ics	
	Steve Shively	David Long	Pat Carrier	Jim Lewis	Bruce Mayer	Ken Bakalar	
	MGC	Scientific Atlanta	MGC	SynthWorks	NGC	MGC	
10:00 - 11:00	Techniques and Tricks: Solving library data problems in DMS	Using I/O Designer for FPGA and PCB Integration	HyperLynx 7.7 Update	Accellera VHDL-2006 Fixed and Floating Point Packages	Accessing Expedition with VB	Design and simulation of an Analog-to-Digital Converter using a Via Configurable Array and ADVance MS	
	Phil Lindberg	Mike Ashbaugh	Pat Carrier	Jim Lewis		James Kemerling	
	APL	Trilogic	MGC	SynthWorks		Triad Semiconductor	
11:00 - 11:30	High-Speed routing methodology in Board Station RE	Mentor Design & Library Translators	Using HyperLynx 7.5 for Planning and Verification of a High-Speed Design	Reaching Deliberate DO-254 compliance with a Random Testbench		Using DXDesigner and Calibre in a mixed Windows/Linux IC design flow	
	Mike Kulkusky	Jim Oakley	Alex Golian	James Keithan		Bruce Mayer	Joel Zolnier
	APL	MGC	NGC	MGC		NGC	Integrated Circuit Designs
11:30-1:00	Lunch / Vendor Visitation						
1:00 - 2:00	Manufacturing Documentation Preparation using FabLink XE		Techniques in Routing High-Speed Designs	Paradox of IP Reuse	The Critical Value of Unconventional Knowledge Sources: Faster Routes to Technical Competence	Introducing the Advanced Verification Methodology (AVM) - Now We're Cookin': Recipes for Advanced Verification	
	Steve Hughes		Ernie Frohring	Dominic Lucido	Jim Edgerton	Tom Fitzpatrick	
	MGC		Trilogic	MGC	MGC	MGC	
2:00 - 3:00	Expedition Enterprise Product Update		IBIS 4.1 and AMS Modeling	Mentor Graphics FPGA Design Tools	Macrovisions's FLEXNet - Hype or Hope?	Questa Codelink: Creating Processor-Driven Testbenches	
	Steve Shively		Pat Carrier	Dan Gardner	Rachel Stanley	Marty Buehring	
	MGC		MGC	MGC	Honeywell	MGC	
3:00-3:30		PADS Product Update	HyperLynx Technology Kits	Advanced design analysis is the key for successful FPGA designs	SupportNet Update	So you want to OOP (Webex)	
		Jim Oakley	Pat Carrier	Dan Gardner	Christine Egli	Mike Mintz	
		MGC	MGC	MGC	MGC	Cisco	
3:30 - 4:00	Vendor Visitation Time						
4:00 - 5:00	Reception						
9:00 - 4:00	Room 9	Mentor Graphics' Usability Lab					