

2005 MARLUG Conference

8:00	Registration and Continental Breakfast						
8:45	Welcome and Announcements - MARLUG Chair						
	RMS 1 & 2	RMS 3 & 4	RM 5	RM 6	RM 7	RM 8	Dining Area
	PADS	Board St / Expedition	High-Speed	FPGA	Functional Verification	Design Env	
9:00 - 10:00	<p style="text-align: center;">Simulating Xilinx Rocket I/O With Hyperlynx GHz</p> <p style="text-align: center;">Ernie Frohring Trilogic</p>	<p style="text-align: center;">SuperMax ECAD Tool</p> <p style="text-align: center;">Timothy Eder Northrop</p>	<p style="text-align: center;">Using Simulation Techniques to Guarantee Successful Backplane Design</p> <p style="text-align: center;">Johnnie Osborne NASA GSFC</p>	<p style="text-align: center;">Single Event Upset Design Techniques for SRAM Based FPGA Devices</p> <p style="text-align: center;">Melanie Berg NASA GSFC</p>	<p style="text-align: center;">Advanced Verification with HDL Designer Series</p> <p style="text-align: center;">Ray Salemi Mentor</p>	<p style="text-align: center;">DMS Essentials: Learning From APL's LMS to DMS Adventure</p> <p style="text-align: center;">Phil Lindberg JHU / APL</p>	<p style="text-align: center;">What's New in Expedition Enterprise – Expanding Your Horizon</p> <p style="text-align: center;">Charles Pfeil Mentor</p>
10:15 - 11:15	<p style="text-align: center;">Using DX Designer & Omnify PLM to Manage ROHS Information</p> <p style="text-align: center;">Chuck McGinley Trilogic</p>	<p style="text-align: center;">All Dimensions Resolved!!</p> <p style="text-align: center;">Al Wainwright Jr. L-3 Comm</p>	<p style="text-align: center;">Methodology using Hyperlynx 7.5 for Planning and Verification</p> <p style="text-align: center;">Alex Golian Northrop</p>	<p style="text-align: center;">Mentor FPGA Design Tools</p> <p style="text-align: center;">Dan Gardner Mentor</p>	<p style="text-align: center;">Assertion-Based Verification with PSL for Quality-Critical Electronic Systems</p> <p style="text-align: center;">Raghu Ardeishar Mentor</p>	<p style="text-align: center;">Welcome to VB for Expedition Automation & DxDesigner</p> <p style="text-align: center;">Bruce Mayer Northrop</p>	
11:30 - 1:30	Lunch						
1:30 - 2:30	<p style="text-align: center;">RoHS Compliance: What Engineers & PCB Designers Need To Know</p> <p style="text-align: center;">Jim Oakley Mentor</p>	<p style="text-align: center;">To_Layout and Beyond - A Tool Story</p> <p style="text-align: center;">Kelli Hosier Northrop</p>	<p style="text-align: center;">High-Speed Update</p> <p style="text-align: center;">Steve McKinney Mentor</p>	<p style="text-align: center;">Synchronous Design Techniques for Reliable Circuitry</p> <p style="text-align: center;">Melanie Berg NASA GSFC</p>	<p style="text-align: center;">Hierarchical Test Benches</p> <p style="text-align: center;">Mary Harris JHU / APL</p>	<p style="text-align: center;">Mentor Graphics New Installation Mechanism</p> <p style="text-align: center;">Jim Luick Mentor</p>	<p style="text-align: center;">What's New in Expedition Enterprise – Expanding Your Horizon</p> <p style="text-align: center;">Charles Pfeil Mentor</p>
2:30 - 3:30	<p style="text-align: center;">PADS Product Update</p> <p style="text-align: center;">Jim Oakley Mentor</p>	<p style="text-align: center;">What's New In Board Station RE -</p> <p style="text-align: center;">Philippe Bridenne Mentor</p>	<p style="text-align: center;">DDR Technology with HyperLynx</p> <p style="text-align: center;">Steve McKinney Mentor</p>	<p style="text-align: center;">Precision Synthesis -- Advanced Synthesis for Complex FPGAs</p> <p style="text-align: center;">Dan Gardner Mentor</p>	<p style="text-align: center;">Eliminate clock-domain crossing errors in RTL with "0-In CDC"</p> <p style="text-align: center;">Chris Rockwood Mentor</p>	<p style="text-align: center;">Getting started with Mentor Graphics board tools on Linux</p> <p style="text-align: center;">Ken Foster Mentor</p>	
4 - 6	Reception						
9 - 4	Mentor Graphics' Usability Lab - Room 9						
10 - 6	Vendor Fair						