

# Printed Circuit Board Design With HDL Designer

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MARLUG - Mid-Atlantic Region Local Users Group  
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# PCB Design With HDL Designer

- ✓ **Motivation**

- **Time savings**
- **Money savings**
- **Simplicity**

- ✓ **Approach**

- **Use single tool for PCB and FPGA design**
- **More FPGA designs than PCB designers**
  - ✓ **Use HDL designer for schematic capture**

# PCB Design With HDL Designer

## Design Process

- v **PCB Design Process (Minimal):**
  - **Schematic Capture**
  - **Displaying Reference Designators and Component Information on Schematic**
  - **Netlist Creation and Conversion**

# PCB Design With HDL Designer

## Schematic Capture - Symbols

- v **Part Symbols**
  - **HDL Symbol Editor**
    - v **Part Name**
    - v **Part Number**
    - v **Package Type**
    - v **Pin Name (or Port Name)**
    - v **Pin Number**

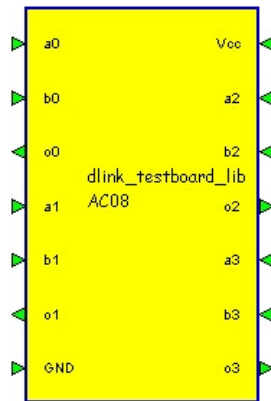
# PCB Design With HDL Designer

## Schematic Capture - Symbols

```
Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
```

### Generic Declarations

```
pin_a0 string "1"
pin_b0 string "2"
pin_o0 string "3"
pin_a1 string "4"
pin_b1 string "5"
pin_o1 string "6"
pin_gnd string "7"
pin_o3 string "8"
pin_b3 string "9"
pin_a3 string "10"
pin_o2 string "11"
pin_b2 string "12"
pin_a2 string "13"
pin_vcc string "14"
part_num string "part_ac08"
pkg_type string "dip14"
```



### Declarations

```
Ports:
GND : IN    std_logic ;
Vcc  : IN    std_logic ;
a0   : IN    std_logic ;
a1   : IN    std_logic ;
a2   : IN    std_logic ;
a3   : IN    std_logic ;
b0   : IN    std_logic ;
b1   : IN    std_logic ;
b2   : IN    std_logic ;
b3   : IN    std_logic ;
o0   : OUT   std_logic ;
o1   : OUT   std_logic ;
o2   : OUT   std_logic ;
o3   : OUT   std_logic ;

User:
```

|                |  |                       |
|----------------|--|-----------------------|
| <company name> |  | <enter comments here> |
|                |  |                       |
|                |  |                       |
|                |  |                       |

# PCB Design With HDL Designer

## Schematic Capture – Schematic Diagrams

- √ **Schematic Diagrams**

- **HDL Block Diagram Editor**

- √ **Part Information from Part Symbol**

- √ **Pin Number**

- √ **Package Type**

- √ **Part Number**

- √ **Connection Information**

- √ **Nets**

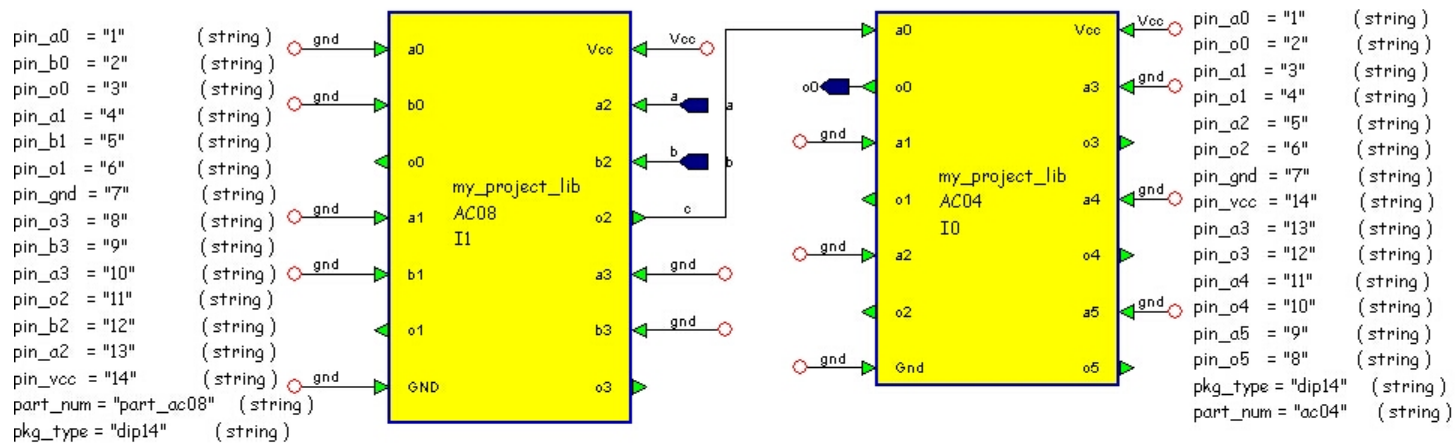
- √ **Reference Designators**

# PCB Design With HDL Designer

## Schematic Capture – Schematic Diagrams

Package List  
 LIBRARY ieee;  
 USE ieee.std\_logic\_1164.all;  
 USE ieee.std\_logic\_arith.all;

Declarations  
 Ports:  
 a : std\_logic  
 b : std\_logic  
 o0 : std\_logic  
 Diagram Signals:  
 SIGNAL Vcc : std\_logic  
 SIGNAL c : std\_logic  
 SIGNAL gnd : std\_logic



|               |              |
|---------------|--------------|
| <tlafourcode> |              |
|               | test circuit |
|               |              |
|               |              |

# PCB Design With HDL Designer

## VHDL Coding

### √ Issue – Where to include Pin Numbers in VHDL?

#### – Comments

- √ Possible

#### – VHDL Attributes

- √ Good Approach but not displayed on Block Diagrams in HDL Designer

#### – VHDL Generics

- √ Chosen Approach but displays pin numbers as a block of text

# PCB Design with HDL Designer

## Netlist Conversion

### v Issue – How can a PADS netlist be produced?

#### —Comments

- v Possible

#### —VHDL Attributes

- v Good Approach but not displayed on Block Diagrams in HDL Designer

#### —VHDL Generics

- v Chosen Approach but displays pin numbers as a block of text

```
GENERIC (  
  pin_a0 : string := "1";  
  pin_o0 : string := "2";  
  pin_a1 : string := "3";  
  pkg_type : string := "dip14";  
  part_num : string := "part_ac04"  
);
```

# Conclusion

- ✓ **Approach can be used PCB design**

- **Would like Vendor to study modifications to HDL Designer**

- ✓ **Schematic Display**

- ✓ **PCB netlist output options**

- ✓ **Design Rule Checking**

- ✓ **Part List Generation**