

Printed Circuit Board Design with HDL Designer

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1 Abstract

Staying up to date with the latest CAD tools both from a cost and time perspective is difficult. Within a given organization there may be experts in Printed Circuit Board Design (PCB) tools and experts in FPGA/VHDL tools. It would be advantageous to utilize expertise in the HDL Designer to design PCBs. This paper describes a limited experiment to do this.

2 PCB Design Process

The PCB design process consists of three phases. Schematic capture, input of component information, and netlist conversion.

3 Schematic Capture

Most designers typically use Mentor Board Station or DxDesigner. These tools have robust front-end schematic capture features. For small applications there may be another alternative. For this project HDL Designer version 2004.1 was used. The HDL Designer block diagram editor was used for schematic capture. The HDL Designer symbol editor created the individual component symbols. This feature allows someone already familiar with the tool to design a PCB. The HDL designer tool can be used in conjunction with the Modelsim simulator for PCB simulation. An FPGA designer can now work under the same simulation environment for the PCB that is currently utilized for the FPGA.

Two part symbols are shown in Figures 1 and 2. Each of these symbols displays the part number, the package type, the layout of the pin numbers, and the signal list. VHDL generics, explained in the next section, were used to hold and display this component information.

Figure 3 is a block diagram or schematic containing two part symbols connected together as well as to VCC and GND. The parts are an AC08 (shown in Figure 2) and an AC04. The reference designators I0 and I1, which are displayed on the schematic, are automatically assigned to the parts by the program.

4 VHDL

The plan is to use VHDL for the PCB netlist format. Very little information explaining how to accomplish this is available. A major effort was taken to standardize VHDL descriptions of not only physical component package information, such as pin and part numbers, but also digital timing, AC, and DC characteristics as well. This standard was eventually abandoned.

Various approaches were studied on how to convey this information into the VHDL net list primarily focusing on pin numbers since that would be essential to the netlist creation. Possible approaches included:

- VHDL comments
- VHDL attributes
- VHDL generics

Although VHDL comments would work, it is more desirable to have this information as part of the language since there may be future extensions to this experiment that would need to use the part information for simulation. The simulator does not read comments.

VHDL user defined attributes were logically a good choice since part information can be used in the component code and passed on to the board schematic. This approach turned out to be unfeasible because HDL designer does not display component attributes on its block diagrams. If these block diagrams are to be used as schematics they must display component pin numbers.

VHDL generics can be displayed on the block diagrams so that approach was chosen. Generics will display the pin numbers as a large block of text rather than on individual ports (see Figure 2).

5 Net list Conversion

PCB layout tools do not usually import VHDL net lists. Even if such a tool did exist there is no standard VHDL netlist format. A typical PADS format was chosen for PCB layout. The challenge is now to take the VHDL net list and convert it to the PADS format. A search for conversion utilities turned up one company that specialized in doing just that. EDAX-NET from Conversion Factors [1] has converted many different formats including VHDL. Their VHDL conversion only assigned part package pin numbers based upon the ordering in the VHDL component declaration. Some of the drawbacks to this approach are:

- Every pin on a part in the component declaration (such as no connects) may not need to be listed.

- Ports need to be listed in the same order in the component declaration and on the part.

- Multiple pin numbers cannot be used for a single port (such as power and ground).

Conversion Factors then modified their utility to eliminate those drawbacks. Their utility now inputs generic mapping information for part pin numbers, part numbers and part package type. This information combined with the port mapping enables EDAX-NET to produce a PADS compatible net list. The test circuit VHDL shown in Figure 3 is listed in Appendix A. The output PADS net list is Appendix B.

5 Conclusion

This study has demonstrated schematic capture using HDL designer and net list conversion to

create a PCB netlist. Two test boards that used HDL Designer are in the design phase. The approach described here is not envisioned as a replacement for current PCB design tools. Such tools have many features. However, some improvements could be made to HDL Designer to make this an attractive alternative to many users. Improvements could be incorporated in schematic display, adding PCB net list output format options, some level of design rule checking, and part list generation.

6 References

[1] Conversion Factors, Inc. 918-825-9300
<http://www.confac.com>

7 Acronyms

CAD	Computer Aided Design
EIA	Electronic Industries Alliance
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
PCB	Printed Circuit Board
VHDL	VHSIC Hardware Description Language
GND	ground
VCC	power
PADS	Mentor Trade Mark

Package List
 LIBRARY ieee;
 USE ieee.std_logic_1164.all;
 USE ieee.std_logic_arith.all;

```

    link_hesboard_lib
    link_sns

Generic declarations
m0_data2 pin_gnd string "1,18,26,28,52,77,79,105,116,129,131,146,157,183,185"
m0_data16 pin_vcc0 string "12,40,60,83,98,115,148,164,167,201"
clk string "19,27,41,76,114,117,130,145,164"
clk_div0 string "2"
clk_div1 string "4"
clk_div2 string "8"
clk_div4 string "16"
clk_div8 string "32"
clk_div16 string "64"
clk_div32 string "128"
clk_div64 string "256"
clk_div128 string "512"
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clk_div512 string "2048"
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clk_div2048 string "8192"
clk_div4096 string "16384"
clk_div8192 string "32768"
clk_div16384 string "65536"
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clk_div65536 string "262144"
clk_div131072 string "524288"
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clk_div524288 string "2097152"
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clk_div8388608 string "33554432"
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clk_div8589934592 string "34359738368"
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clk_div137438953472 string "549755813888"
clk_div274877906944 string "1099511627776"
clk_div549755813888 string "2199023255552"
clk_div1099511627776 string "4398046511104"
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clk_div35184372088832 string "140737488355328"
clk_div70368744177664 string "281474976710656"
clk_div140737488355328 string "562949953421312"
clk_div281474976710656 string "1125899906842624"
clk_div562949953421312 string "2251799813685248"
clk_div1125899906842624 string "4503599627370496"
clk_div2251799813685248 string "9007199254740992"
clk_div4503599627370496 string "18014398509481984"
clk_div9007199254740992 string "36028797018963968"
clk_div18014398509481984 string "72057594037927936"
clk_div36028797018963968 string "144115188075855872"
clk_div72057594037927936 string "288230376151711744"
clk_div144115188075855872 string "576460752303423488"
clk_div288230376151711744 string "1152921504606846976"
clk_div576460752303423488 string "2305843009213693952"
clk_div1152921504606846976 string "4611686018427387904"
clk_div2305843009213693952 string "9223372036854775808"
clk_div4611686018427387904 string "18446744073709551616"
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clk_div2417851639229258349412352 string "9671406556917033397649408"
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clk_div154742504910672534362390528 string "618970019642690137449562112"
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clk_div5846006549428815721819163251991159126104444608 string "23384026197715262887276653007964764504177824"
clk_div11692013098857631443638326503982382252088912 string "46768052395430525774553306015929529008355456"
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clk_div93536104790861051549106612031858058016711112 string "374144419163444206196426480074332240444448"
clk_div187072209581722103098213224037166160233422224 string "748288838326888412392852960148664480888896"
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clk_div153249554089346748457816575984474444608 string "6129982163573869938312663839378978242432"
clk_div30649910817869349691563319196894889121216 string "12259964327147738776625327678757956484864"
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clk_div49039857308590955106501310715031825939552 string "19615942923436382042600522860012303755776"
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clk_div19615942923436382042600522860012303755776 string "78463771693745528170402091440048150311104"
clk_div39231885846872764085201045720024607515552 string "156927543387491056340804182800096300622208"
clk_div78463771693745528170402091440048150311104 string "313855086774982112680608365600192601244416"
clk_div156927543387491056340804182800096300622208 string "627710173549964225361216731200385202488832"
clk_div313855086774982112680608365600192601244416 string "12554203470999284507224346240077040489776"
clk_div627710173549964225361216731200385202488832 string "2510840694199856901444869248001540975552"
clk_div12554203470999284507224346240077040489776 string "5021681388399713802889738496003081951104"
clk_div2510840694199856901444869248001540975552 string "1004336277679942760577947699200616382208"
clk_div5021681388399713802889738496003081951104 string "20086725553598855211558953984001227664512"
clk_div10043
```

```

Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

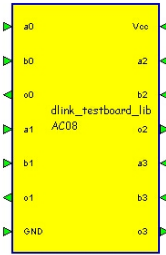
```

Generic Declarations

```

pin_a0 string "1"
pin_b0 string "2"
pin_o0 string "3"
pin_a1 string "4"
pin_b1 string "5"
pin_o1 string "6"
pin_gnd string "7"
pin_o3 string "8"
pin_b3 string "9"
pin_a3 string "10"
pin_o2 string "11"
pin_b2 string "12"
pin_a2 string "13"
pin_vcc string "14"
part_num string "part_ac08"
pkg_type string "dip14"

```



Declarations

```

Ports:
GND : IN    std_logic ;
Vcc  : IN    std_logic ;
a0   : IN    std_logic ;
a1   : IN    std_logic ;
a2   : IN    std_logic ;
a3   : IN    std_logic ;
b0   : IN    std_logic ;
b1   : IN    std_logic ;
b2   : IN    std_logic ;
b3   : IN    std_logic ;
o0   : OUT   std_logic ;
o1   : OUT   std_logic ;
o2   : OUT   std_logic ;
o3   : OUT   std_logic ;
User:

```

Figure 2.

<company name>	
<enter comments here>	

Figure 3.

```

Package List
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

```

```

Declarations
Ports:
a : std_logic
b : std_logic
o0 : std_logic

```

```

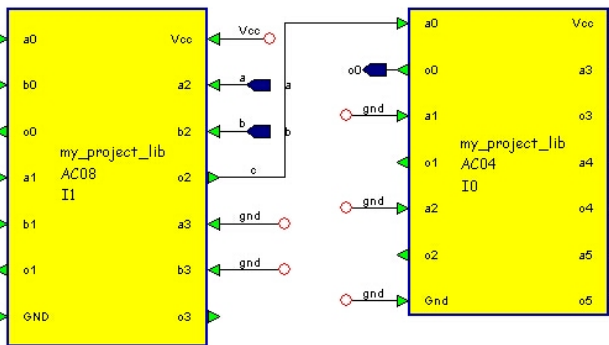
Diagram Signals:
SIGNAL Vcc : std_logic
SIGNAL c : std_logic
SIGNAL gnd : std_logic

```

```

pin_a0 = "1" (string)
pin_b0 = "2" (string)
pin_o0 = "3" (string)
pin_a1 = "4" (string)
pin_b1 = "5" (string)
pin_o1 = "6" (string)
pin_gnd = "7" (string)
pin_o3 = "8" (string)
pin_b3 = "9" (string)
pin_a3 = "10" (string)
pin_o2 = "11" (string)
pin_b2 = "12" (string)
pin_a2 = "13" (string)
pin_vcc = "14" (string)
part_num = "part_ac08" (string)
pkg_type = "dip14" (string)

```



```

pin_a0 = "1" (string)
pin_o0 = "2" (string)
pin_a1 = "3" (string)
pin_o1 = "4" (string)
pin_a2 = "5" (string)
pin_o2 = "6" (string)
pin_gnd = "7" (string)
pin_vcc = "14" (string)
pin_a3 = "13" (string)
pin_o3 = "12" (string)
pin_a4 = "11" (string)
pin_o4 = "10" (string)
pin_a5 = "9" (string)
pin_o5 = "8" (string)
pkg_type = "dip14" (string)
part_num = "ac04" (string)

```

<tlafourcade>	
test circuit	

Appendix A

```
-- VHDL Entity my_project_lib.test_ckt.symbol
--
-- Created:
--   by - tlfourca (TERESANT1)
--
-- Generated by Mentor Graphics' HDL Designer(TM) 2004.1
--
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

ENTITY test_ckt IS
  PORT(
    a : IN  std_logic;
    b : IN  std_logic;
    o0 : OUT std_logic
  );

-- Declarations

END test_ckt ;

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

ARCHITECTURE struct OF test_ckt IS

  -- Internal signal declarations
  SIGNAL Vcc : std_logic;
  SIGNAL c  : std_logic;
  SIGNAL gnd : std_logic;

  -- Component Declarations
  COMPONENT AC04
  GENERIC (
    pin_a0 : string := "1";
    pin_o0 : string := "2";
    pin_a1 : string := "3";
    pin_o1 : string := "4";
    pin_a2 : string := "5";
    pin_o2 : string := "6";
    pin_gnd : string := "7";
    pin_vcc : string := "14";
    pin_a3 : string := "13";
    pin_o3 : string := "12";
    pin_a4 : string := "11";
    pin_o4 : string := "10";
    pin_a5 : string := "9";
    pin_o5 : string := "8";
    pkg_type : string := "dip14";
    part_num : string := "part_ac04"
  );
  PORT (
    Gnd : IN  std_logic ;
    Vcc : IN  std_logic ;
    a0 : IN  std_logic ;
    a1 : IN  std_logic ;
    a2 : IN  std_logic ;
```

```

a3 : IN  std_logic ;
a4 : IN  std_logic ;
a5 : IN  std_logic ;
o0 : OUT std_logic ;
o1 : OUT std_logic ;
o2 : OUT std_logic ;
o3 : OUT std_logic ;
o4 : OUT std_logic ;
o5 : OUT std_logic
);
END COMPONENT;
COMPONENT AC08
GENERIC (
  pin_a0 : string := "1";
  pin_b0 : string := "2";
  pin_o0 : string := "3";
  pin_a1 : string := "4";
  pin_b1 : string := "5";
  pin_o1 : string := "6";
  pin_gnd : string := "7";
  pin_o3 : string := "8";
  pin_b3 : string := "9";
  pin_a3 : string := "10";
  pin_o2 : string := "11";
  pin_b2 : string := "12";
  pin_a2 : string := "13";
  pin_vcc : string := "14";
  part_num : string := "part_ac08";
  pkg_type : string := "dip14"
);
PORT (
  GND : IN  std_logic ;
  Vcc : IN  std_logic ;
  a0 : IN  std_logic ;
  a1 : IN  std_logic ;
  a2 : IN  std_logic ;
  a3 : IN  std_logic ;
  b0 : IN  std_logic ;
  b1 : IN  std_logic ;
  b2 : IN  std_logic ;
  b3 : IN  std_logic ;
  o0 : OUT std_logic ;
  o1 : OUT std_logic ;
  o2 : OUT std_logic ;
  o3 : OUT std_logic
);
END COMPONENT;

```

BEGIN

```

-- Instance port mappings.
I0 : AC04

```

```

PORT MAP (
  Gnd => gnd,
  Vcc => Vcc,
  a0 => c,
  a1 => gnd,
  a2 => gnd,
  a3 => gnd,
  a4 => gnd,
  a5 => gnd,

```

```
o0 => o0,  
o1 => OPEN,  
o2 => OPEN,  
o3 => OPEN,  
o4 => OPEN,  
o5 => OPEN  
);  
I1 : AC08  
PORT MAP (  
  GND => gnd,  
  Vcc => Vcc,  
  a0 => gnd,  
  a1 => gnd,  
  a2 => a,  
  a3 => gnd,  
  b0 => gnd,  
  b1 => gnd,  
  b2 => b,  
  b3 => gnd,  
  o0 => OPEN,  
  o1 => OPEN,  
  o2 => c,  
  o3 => OPEN  
);  
END struct
```

Appendix B

PADS-LOGIC*

REMARK created with EDAX-NET V7.0.3

REMARK

PART

I0 PART_AC04,AC04@DIP14

I1 PART_AC08,AC08@DIP14

NET

SIGNAL GND

I0.7 I0.3 I0.5 I0.13 I0.11 I0.9 I1.7 I1.1

I1.4 I1.10 I1.2 I1.5 I1.9

SIGNAL VCC

I0.14 I1.14

SIGNAL C

I0.1 I1.11

SIGNAL O0

I0.2

SIGNAL A

I1.13

SIGNAL B

I1.12

END OF ASCII OUTPUT FILE