

Checking Vendor IBIS Models Using Hyperlynx Visual IBIS Editor October 2004

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MARLUG - Mid-Atlantic Region Local Users Group
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Agenda

- ✓ **IBIS Background**
- ✓ **IBIS Model Basics**
- ✓ **Visual IBIS Editor**
- ✓ **Steps to Checking the IBIS Model**
- ✓ **Errors and Warnings**
- ✓ **Testing the IBIS Model in LineSim**
- ✓ **Assigning Library Models Automatically**

IBIS Background

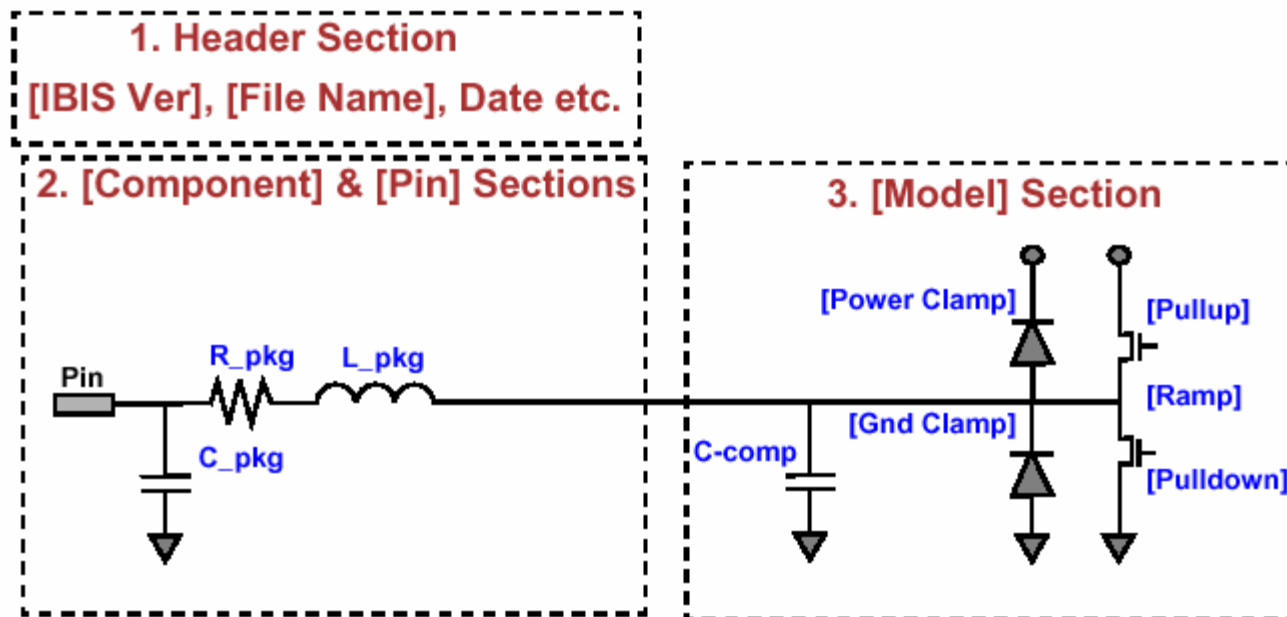
- v **What is IBIS? (I/O Buffer Information Spec.)**
 - Standard for describing analog behavior of the buffers of digital devices specifically for signal integrity analysis
- v **Originated at Intel early '90's for PCI bus signal integrity 'what-if' analysis**
 - Started as behavioral buffer model in HSpice

IBIS Background

- ✓ **Became a tool independent common modeling format using ASCII formatted text data**
- ✓ **With the support of many vendors, the IBIS Open Forum formed and IBIS specification written (first release 1993)**
- ✓ **Models generated through SPICE translation or actual device measurements**

Parts of an IBIS file

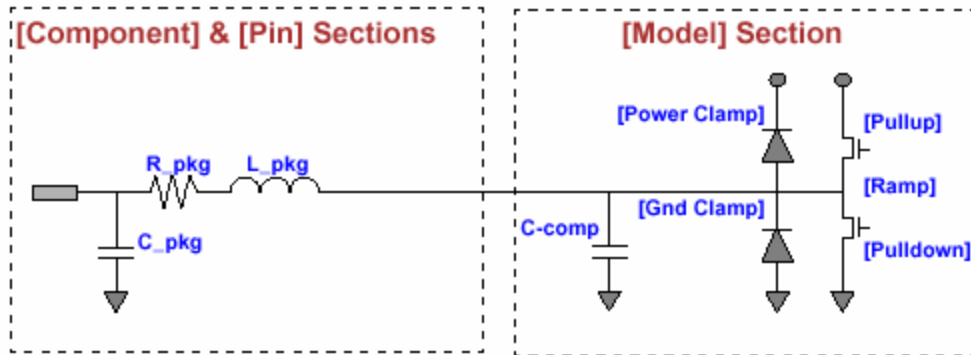
- v All models consist of 3 sections:
 - Header : information about the model
 - Component : describes the component name, pinouts and package parasitics
 - Model : describes the behavior of each buffer



Source: ICX Modeling Guide V3.3

BASIC IBIS MODEL

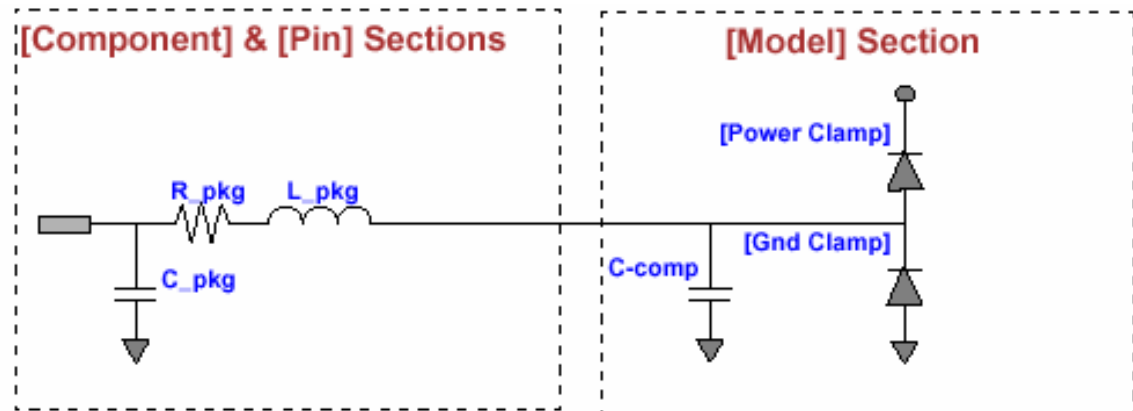
Driver Model Schematic



A basic IBIS model consists of:

- four I-V curves:
 - pullup & POWER clamp
 - pulldown & GND clamp
 - two ramps:
 - dV/dt_{rise}
 - dV/dt_{fall}
 - die capacitance:
 - C_{comp}
 - packaging:
 - RLC values
- for each buffer on a chip**

Receiver Model Schematic



Source: ICX Modeling Guide V3.3

Four I-V Curves of IBIS Model

- ✓ **[Pulldown], referenced to [Pulldown Reference]**
 - Contains the difference of drive and receive (3-state) mode I-V curves for driver driving low
 - Curve Origin usually at 0V

- ✓ **[Pullup], referenced to [Pullup Reference]**
 - Contains the difference of drive and receive (3-state) mode I-V curves for driver driving high
 - Curve Origin usually at supply voltage

Source: *Introduction to IBIS Models and IBIS Model Making*

Four I-V Curves of IBIS Model (cont.)

- v **[GND Clamp], referenced to [GND Clamp Reference]**
 - Contains the receive (3-state) mode I-V curves
 - Curve Origin usually at 0V

- v **[POWER Clamp], referenced to [POWER Clamp Reference]**
 - Contains the receive (3-state) mode I-V curves
 - Curve Origin usually at supply voltage

Source: *Introduction to IBIS Models and IBIS Model Making*

Hyperlynx Visual IBIS Editor

v 3 View Windows

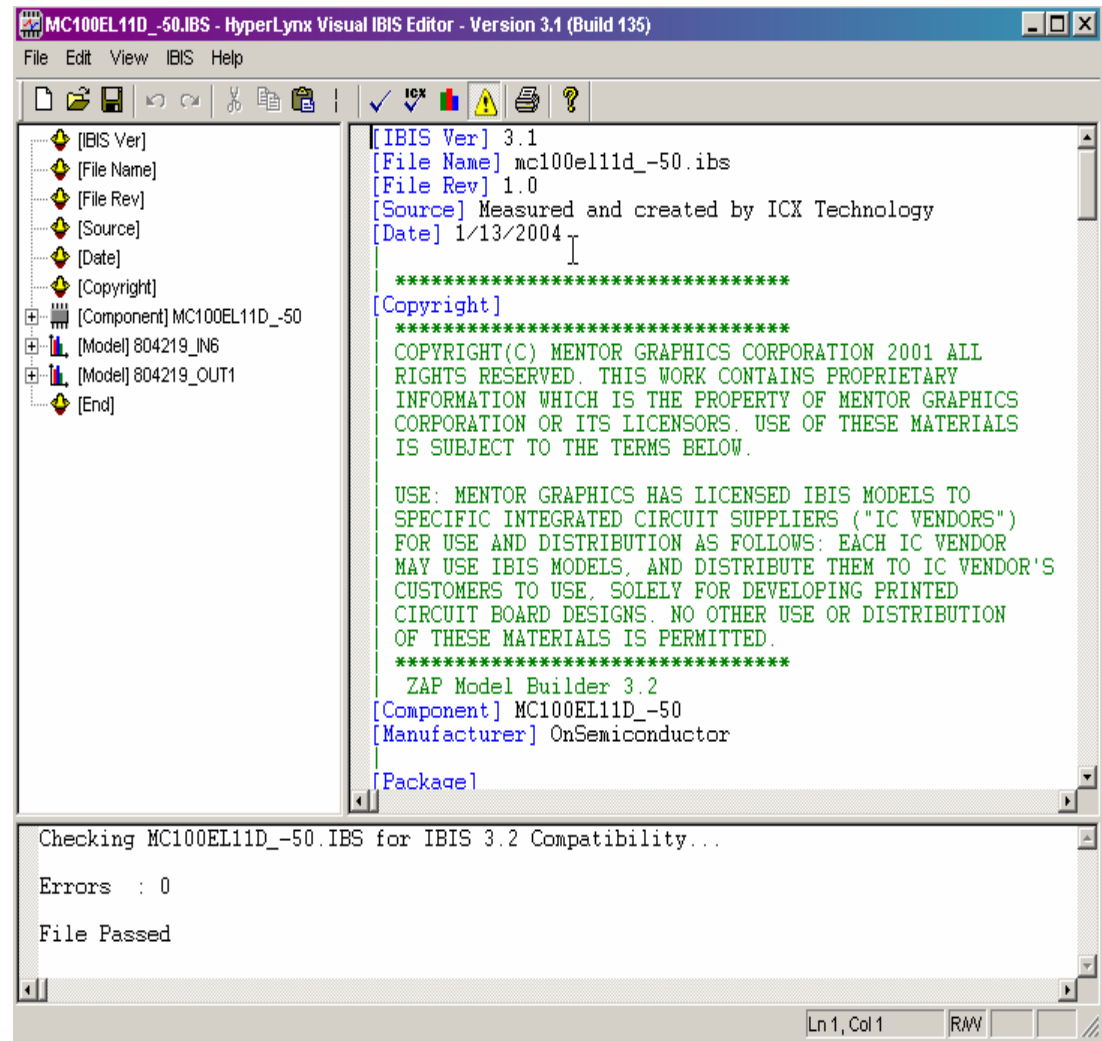
- Tree-View Pane
- Main Edit Window
- Output Window

v Performs Syntax Checking

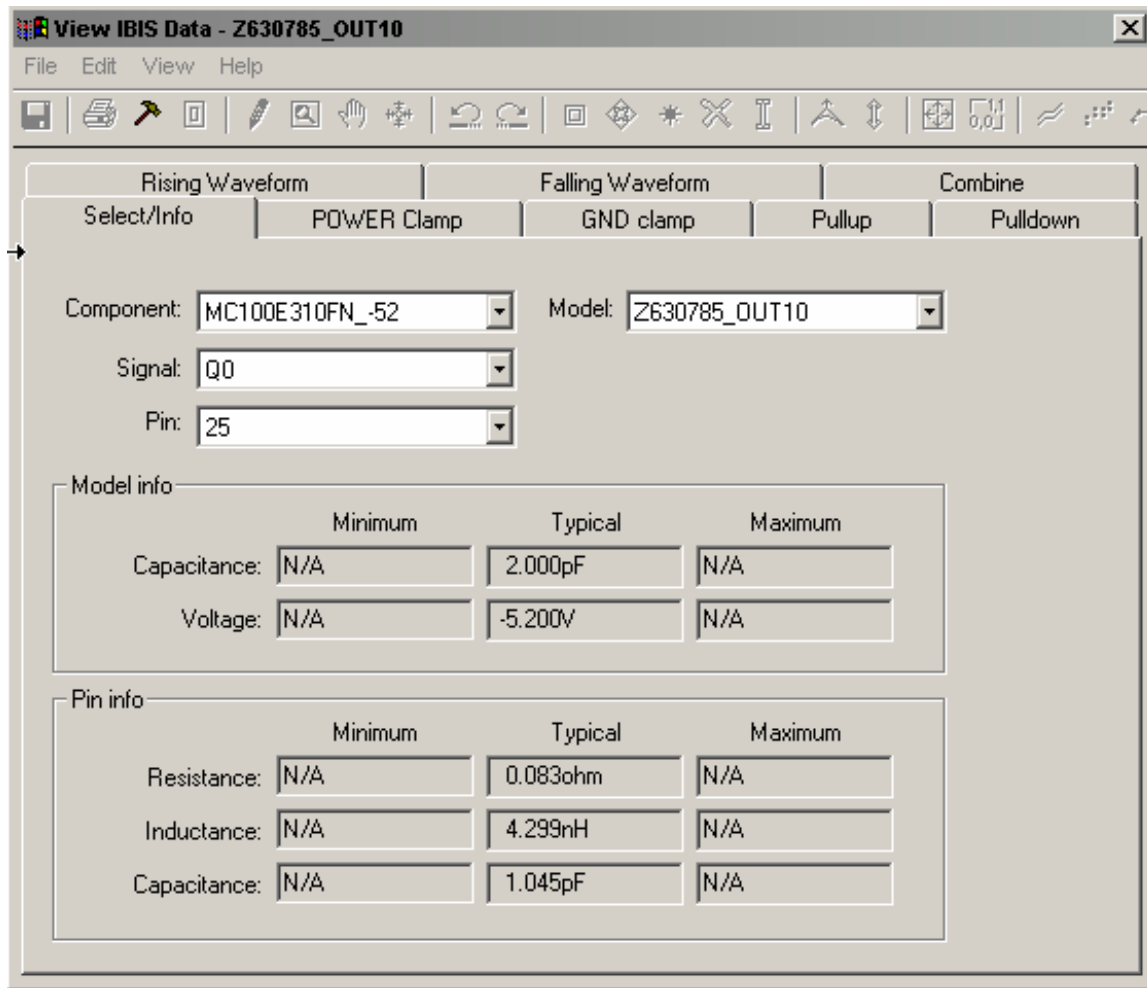
- IBIS Committee parser (up to ver. 3.2)
- ICX parser

v Graphical Data View

- View Data (V/I curves)
- View Data (V/T curves)
- View Data (Part Info)



Visual IBIS Data Window



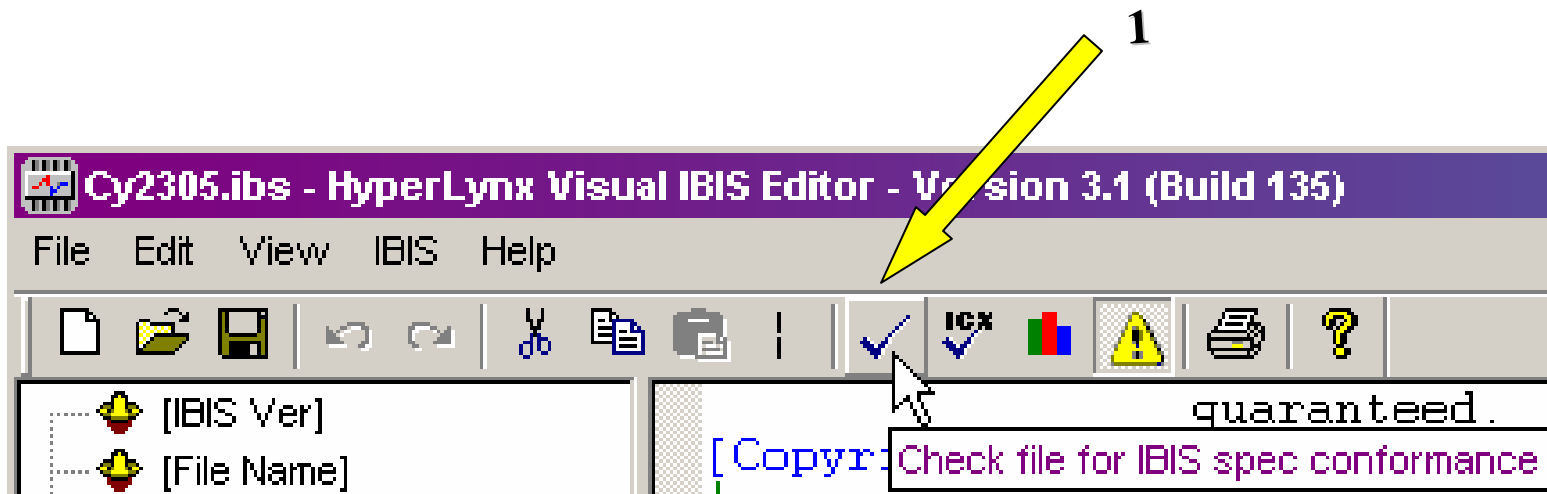
v Provides easy access to

- model info
- V/I curves
- V/T curves
- Die capacitance
- Pin characteristics

Source: Hyperlynx 7.1

Steps to Check the Model

1. **Verify Syntax of IBIS file (F9)**
 - IBIS committee parser (version specific) run on file
 - ICX parser available if ICX 3.1 or newer installed
2. Visually Check Curves
3. Test IBIS Model in Hyperlynx LineSim



Syntax Errors and Warnings

v Errors & Warnings displayed in Output window

```
Checking Cy2305.ibs for IBIS 2.1 Compatibility...  
WARNING (line 26) - Typ value is not in between Min and Max  
WARNING (line 47) - Vinl should not be specified for model type 3-state  
WARNING (line 48) - Vinh should not be specified for model type 3-state  
WARNING (line 59) - Pulldown Typical data is non-monotonic  
WARNING (line 59) - Pulldown Minimum data is non-monotonic  
WARNING (line 70) - Pulldown Maximum data is non-monotonic  
WARNING (line 136) - Pullup Minimum data is non-monotonic  
WARNING (line 137) - Pullup Typical data is non-monotonic  
WARNING (line 148) - Pullup Maximum data is non-monotonic  
WARNING - Model Buffer1: POWER Clamp : Typical value never becomes zero  
WARNING - Model Buffer1: POWER Clamp : Minimum value never becomes zero  
WARNING - Model Buffer1: POWER Clamp : Maximum value never becomes zero  
WARNING - Model Input1: GND Clamp : Maximum value never becomes zero  
  
Errors : 0  
Warnings: 13  
  
File Passed
```

- v **Simulators will accept models with warning-level violations, but may produce incorrect results!**
- v **Errors may prevent simulator from running or produce unusual results.**

Resolving Errors and Warnings

Example: Typical Value not between Min and Max

The screenshot shows the Hyperlynx Visual IBIS Editor interface. On the left is a project tree with components like [Component] cy2305 and [Model] Buffer1. The main window displays the component's parameters in a table format. The 'C_pkg' parameter is highlighted, and its typical value '340.00fF' is circled in red. Below the table, a warning message is displayed: 'WARNING (line 26) - Typ value is not in between Min and Max'.

variable	typ	min	max
R_pkg	46.00m	40.00m	52.00m
L_pkg	5.00nH	3.10nH	7.10nH
C_pkg	340.00fF	510.00fF	980.00fF

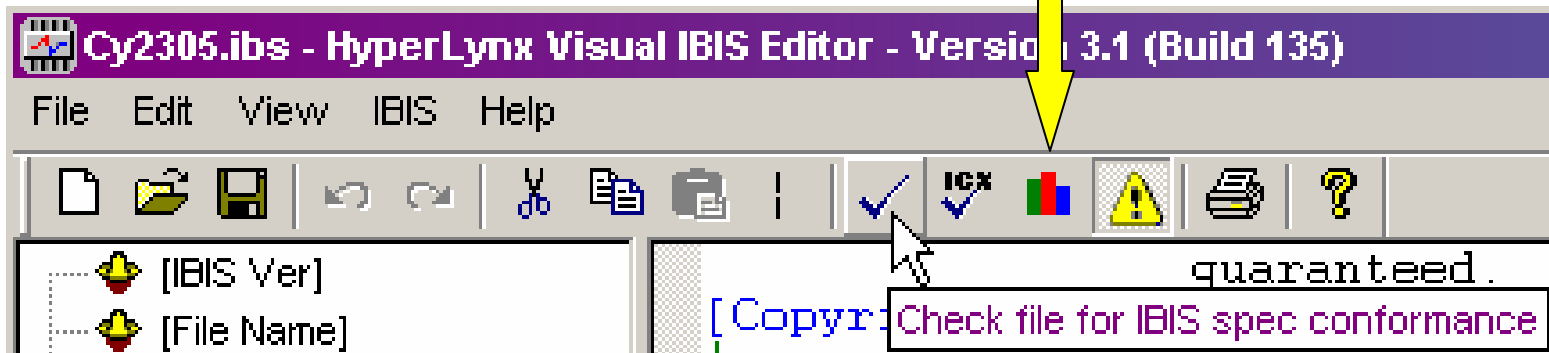
[Pin]	signal_name	model_name	R_pin	L_pin
2	CLK2	Buffer1		
3	CLK1	Buffer1		
5	CLK3	Buffer1		
7	CLK4	Buffer1		
8	CLKOUT	Buffer1		

Checking Cy2305.ibs for IBIS 2.1 Compatibility...

- WARNING (line 26) - Typ value is not in between Min and Max
- WARNING (line 47) - Vinl should not be specified for model type 3-state

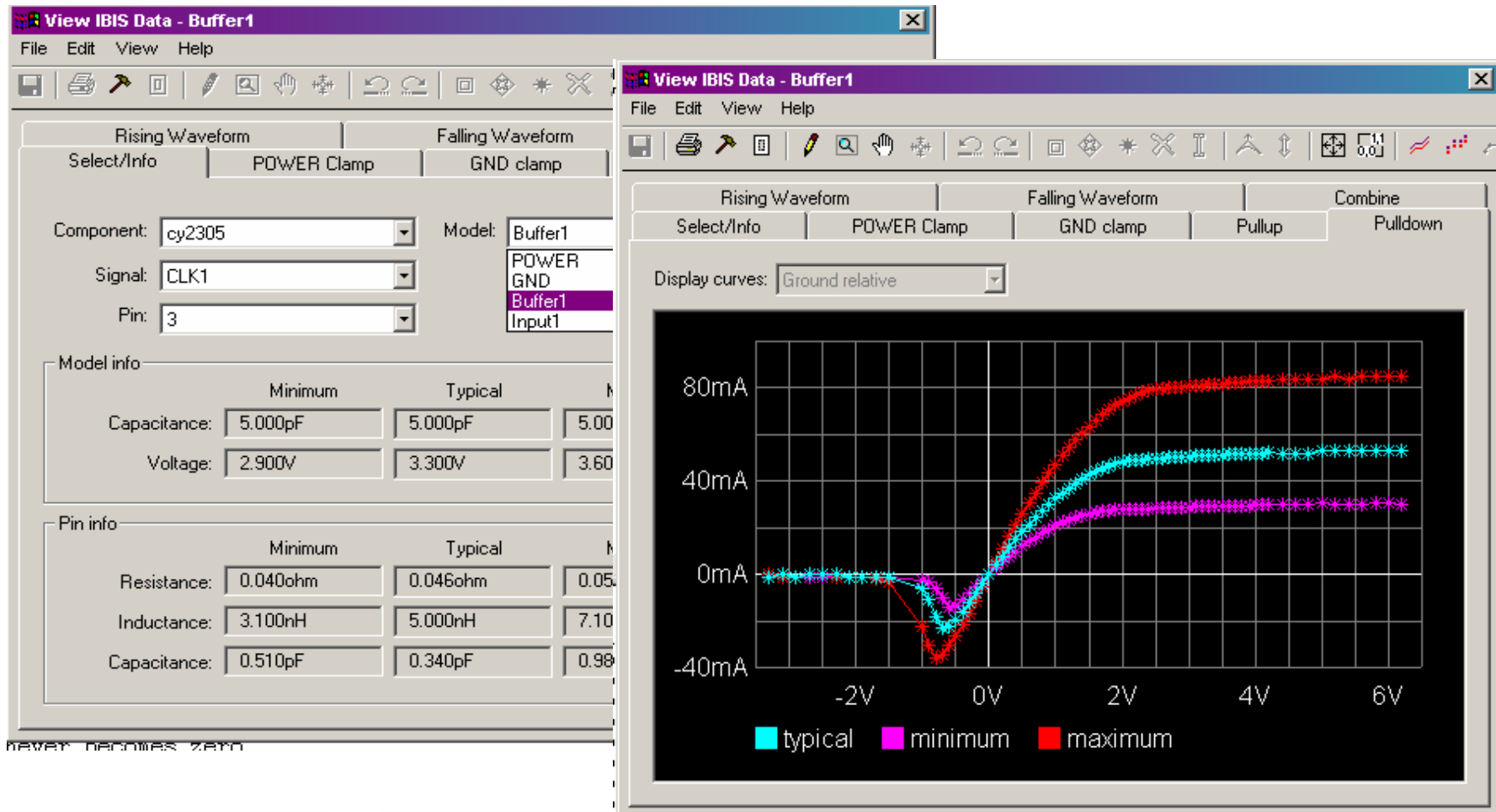
Steps to Check the Model

1. Verify Syntax of IBIS file (F9)
2. Visually Check V-I curves
 - Non-monotonicity
 - Wrong sign
 - Bad numeric values
 - Noise
3. Test IBIS Model in LineSim



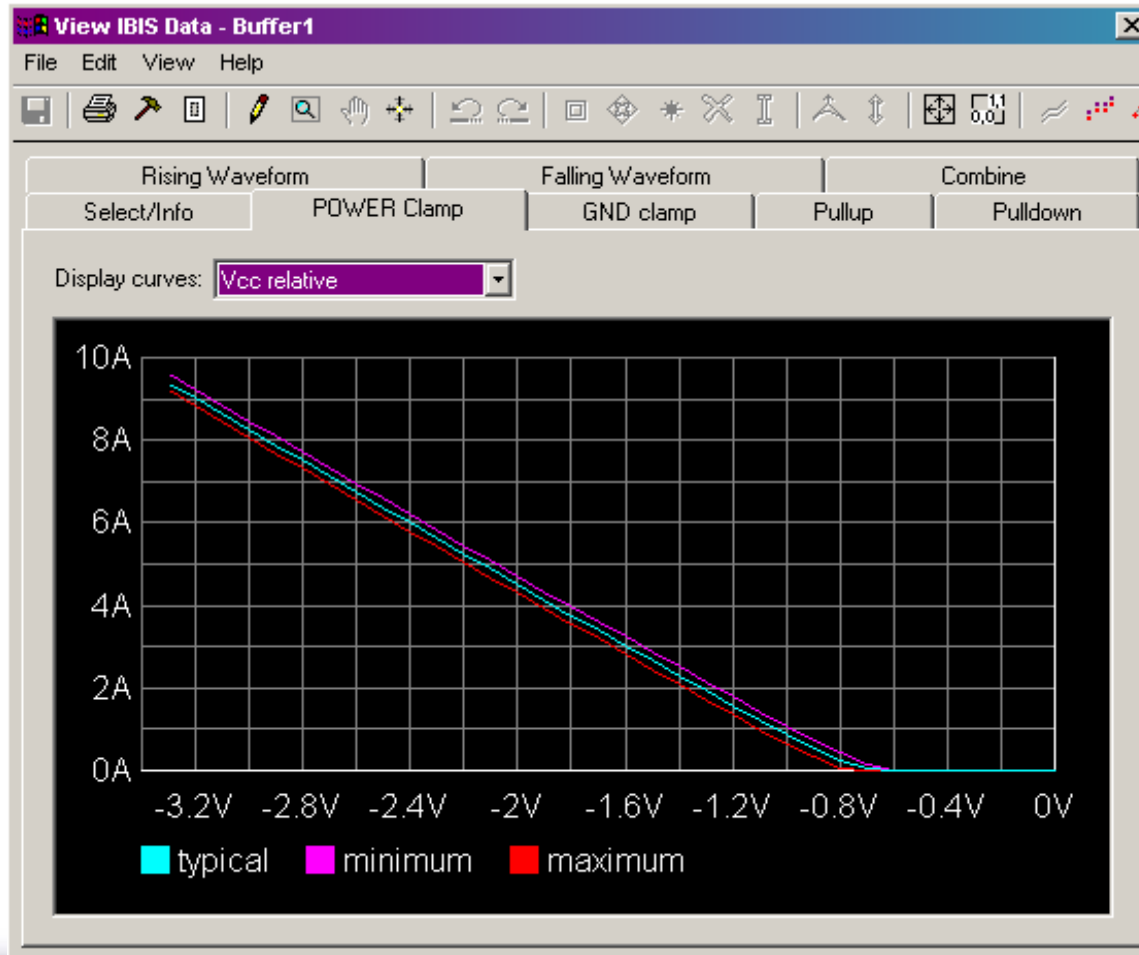
Resolving Errors and Warnings

Non-monotonic Warning



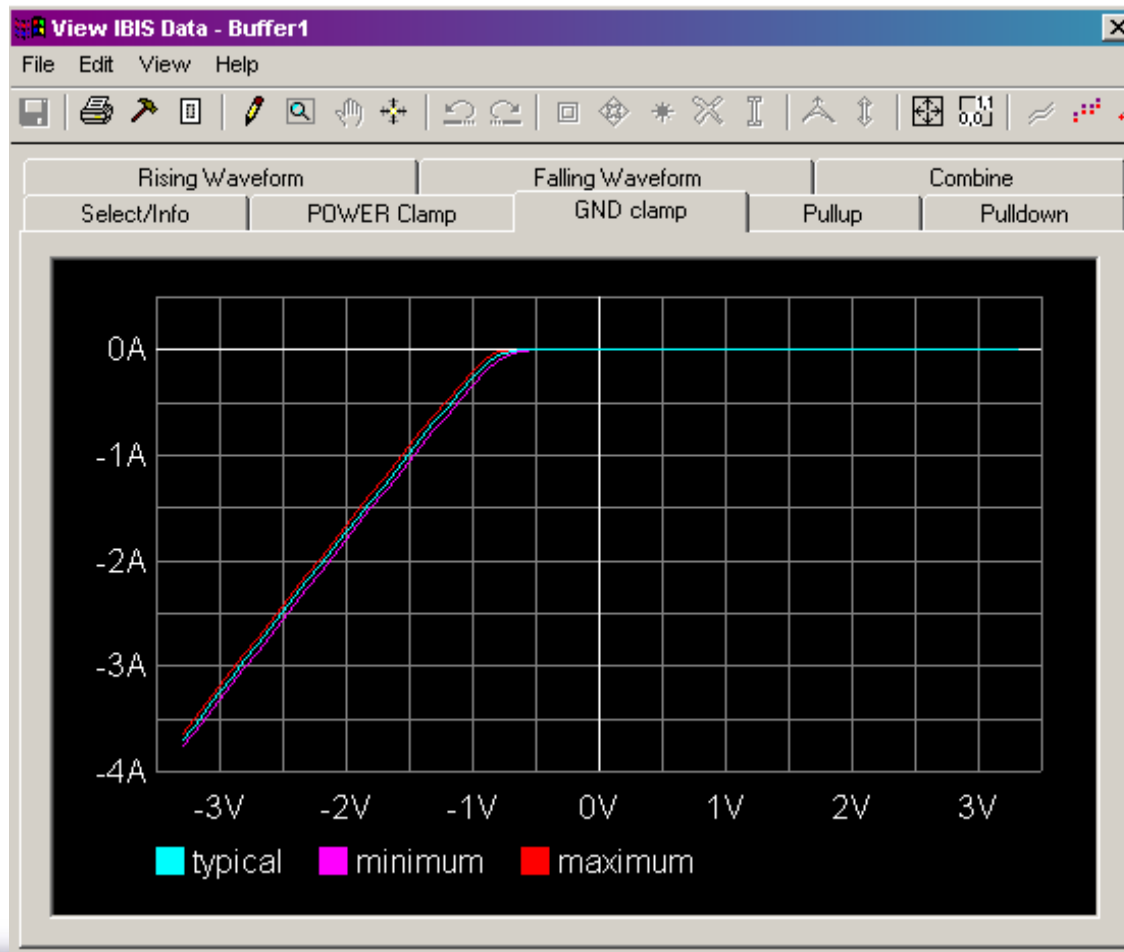
Resolving Errors and Warnings

- ✓ **POWER Clamp** – value never becomes zero



Resolving Errors and Warnings

- ✓ **GND Clamp** – value never becomes zero

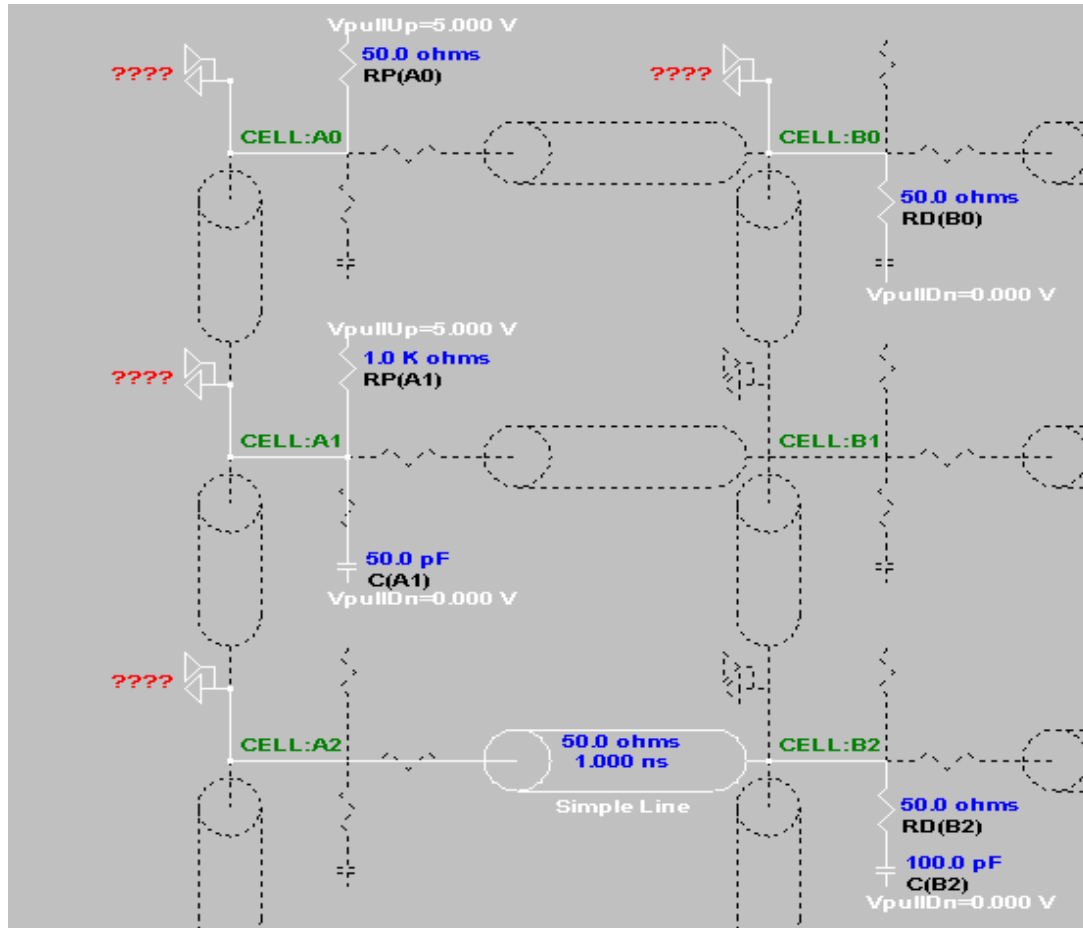


3. Test IBIS Model in LineSim

- ✓ Use Hyperlynx LineSim to check that driver will drive recommended loads
- ✓ 2 test circuits exist in HYPFILES folder
 - IBISTest.TLN (for single-ended driver)
 - IbisDiff.tln (for differential driver)
 - Modify loads for ECL drivers with pulldown to Vtt
 - Modify loads for open drain drivers with pullup to Vtt
- ✓ Assign your IBIS model to all outputs in schematic
- ✓ Open Oscilloscope and **Start Simulation** (allow Oscilloscope to automatically assign scope probes)
- ✓ Determine whether results are acceptable

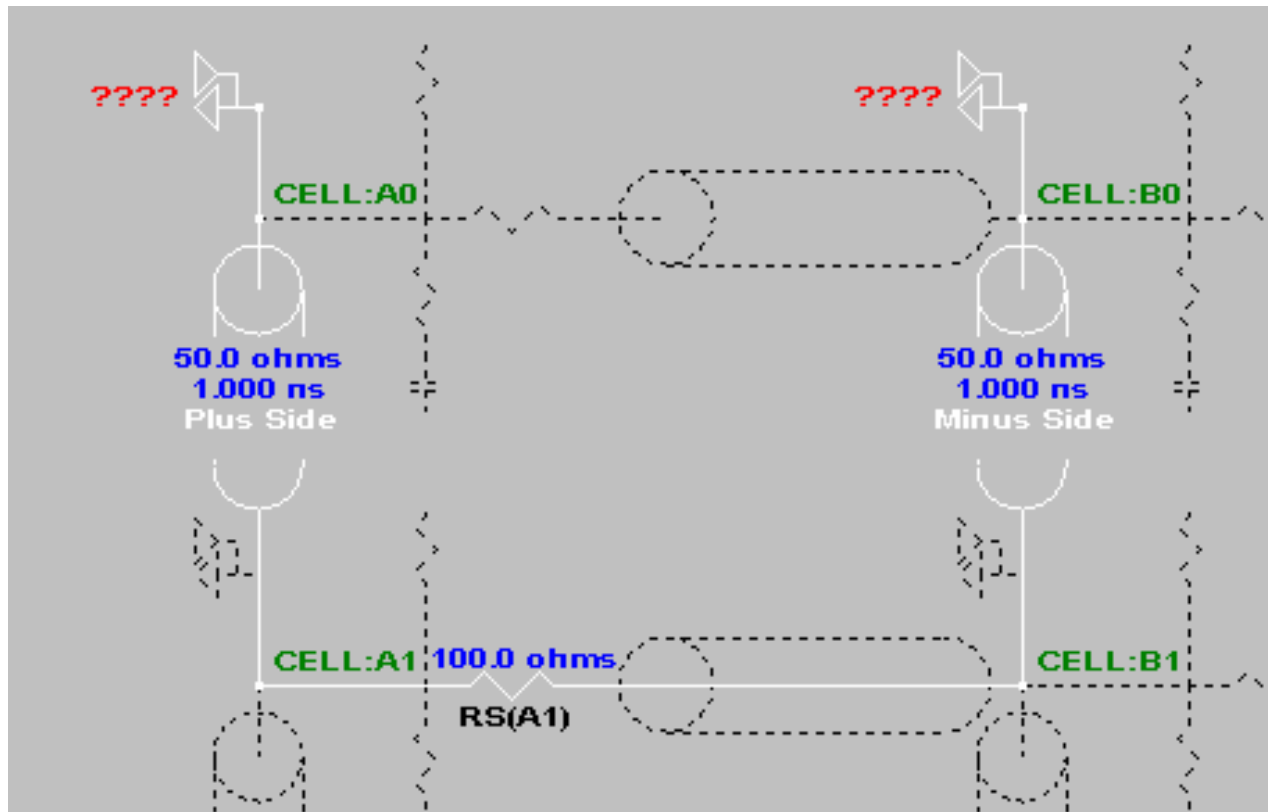
Verification: LineSim Test Circuits

v IBISTest.TLN



Verification: LineSim Test Circuits

v IbisDiff.tln



Assigning Library Models Automatically

- ✓ **Hyperlynx and ICX design files can have IBIS models defined from properties on schematic symbols in the design**

- ✓ **ICX uses:**
 - **ICX_PART_MODEL - [component] within IBIS file**
 - **ICX_TECH – default model to use if IBIS model is unavailable**

- ✓ **Hyperlynx* uses:**
 - **HYP_LIB – identifies the IBIS filename**
 - **HYP_DEVICE – [component] within IBIS file**

***Properties are new as of version 7.2**

Assigning Library Models Automatically

- ✓ **Each tool must have paths setup to the locations of the IBIS files**

- ✓ **ICX uses an environment variable:**
 - **ICX_IBIS_SEARCH_PATH**
 - **Set the value to IBIS file directories**
 - **Path only needs to be to a top-level dir**

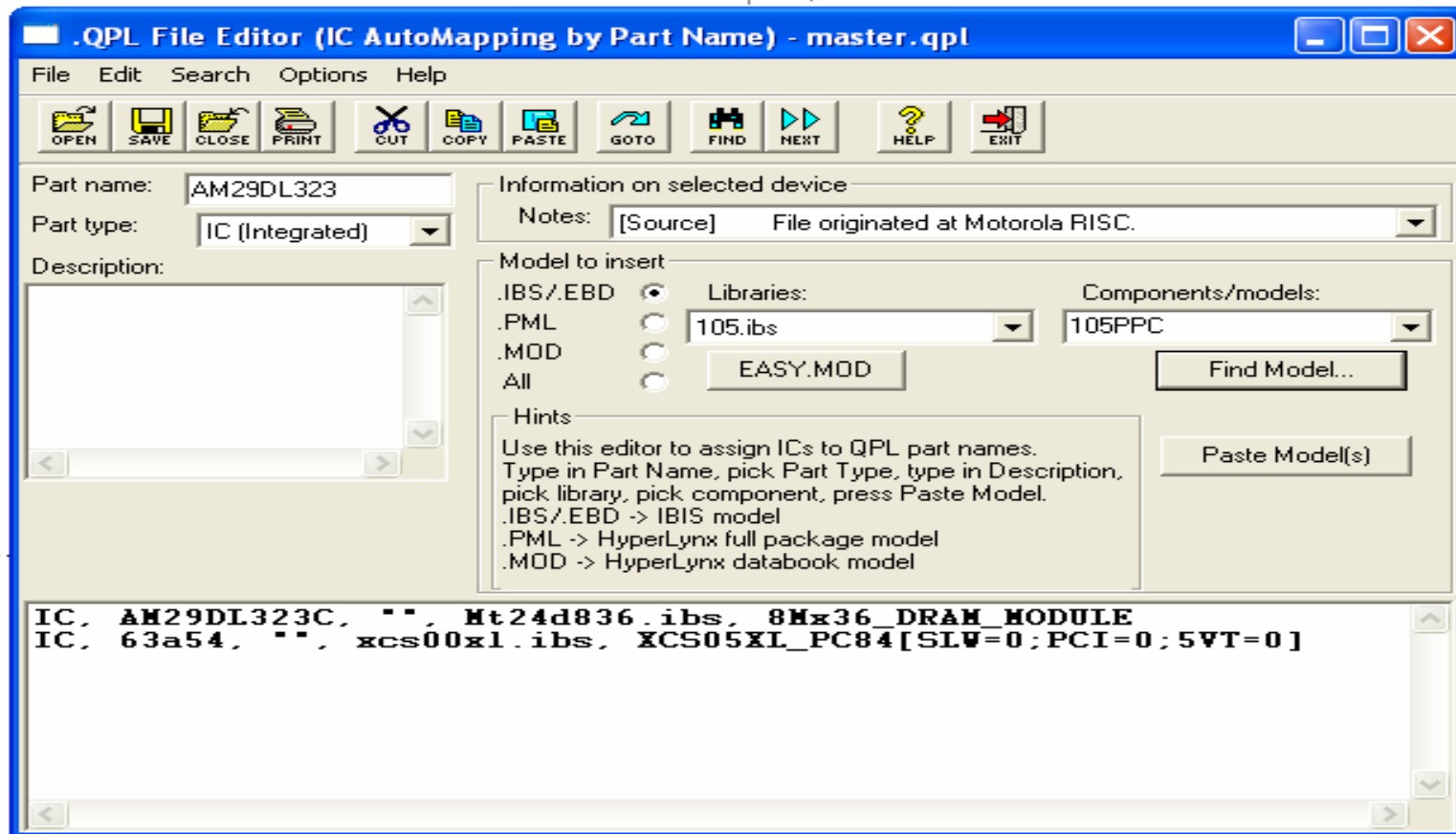
- ✓ **Hyperlynx requires you to add hard paths to the IBIS library files using the menu selection**
 - **Options > Directories...**
 - **Path must be to exact file location**

Assigning Library Models Automatically

- v **An alternate method in Hyperlynx BoardSim:**
 - **Assign models using QPL file for IC's and REF file for discretetes**
 - 1) Create a master QPL file
 - 2) Associate Comp property with models using the .QPL File Editor
 - 3) Turn on the “Use QPL file to assign models” option from the Set Directories dialog box
 - 4) REF file created in LAYOUT using Mentor custom ample code

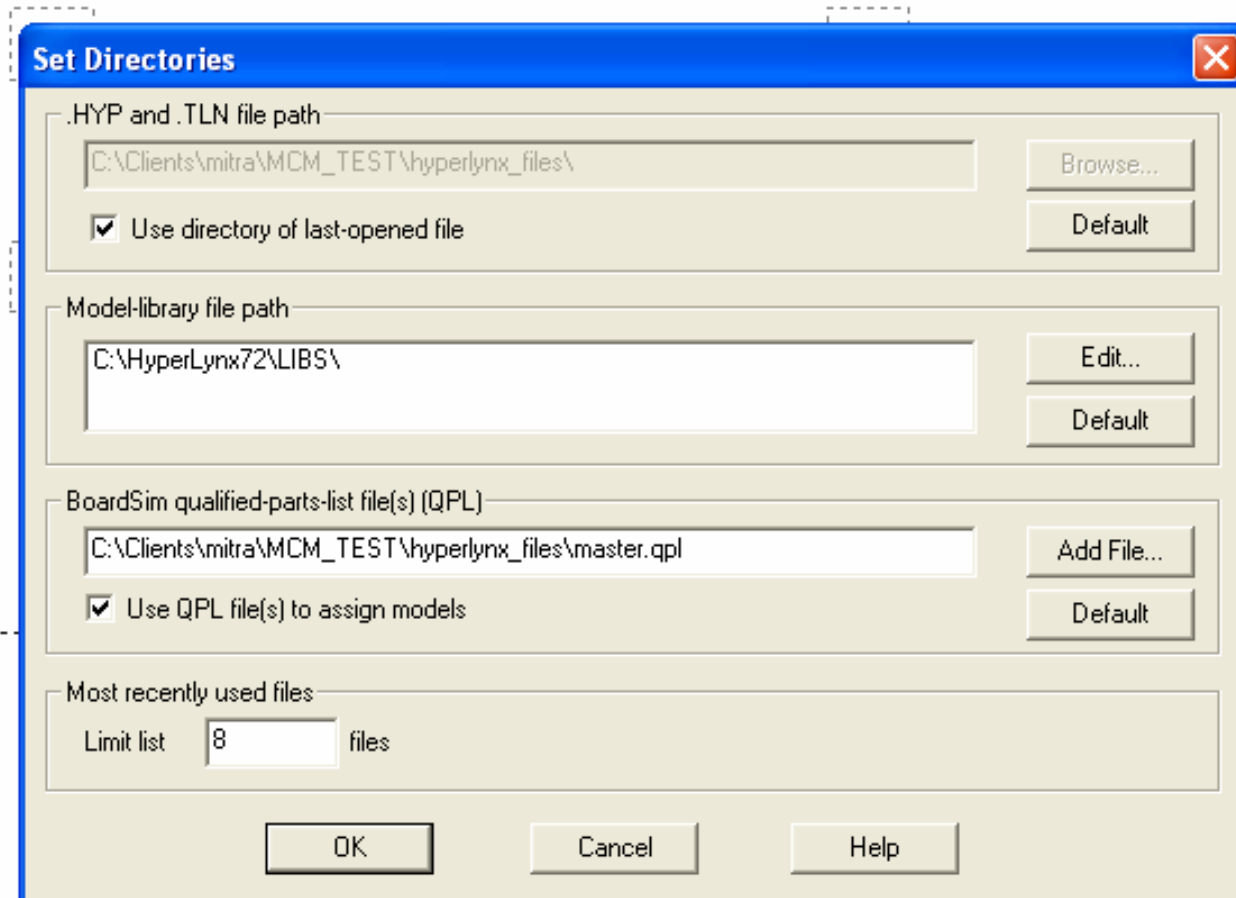
Assigning Library Models Automatically

Edit > QPL Automapping File



Assigning Library Models Automatically

v Options > Directories..



Summary

- ✓ **Hyperlynx Visual IBIS Editor simplifies the checking of IBIS model files by providing both syntax checking and visual curve editing in one tool.**
- ✓ **The 3 step checking approach described herein can be used as a validation process to populate a “controlled” IBIS library for design re-use.**
- ✓ **Both ICX and Hyperlynx provide means to have IBIS models automatically assigned to your SI design file.**

References

- ✓ **Hyperlynx On-line Help Manuals**
- ✓ **ICX Modeling Guide v. 3.3**
- ✓ **Introduction to IBIS Models and IBIS Model Making, Arpad Muranyi, Intel Corp. (Nov 2003)**
- ✓ **Effective Signal Integrity Analysis Using IBIS Models, Syed B. Huq, Cisco Systems, Inc.**

