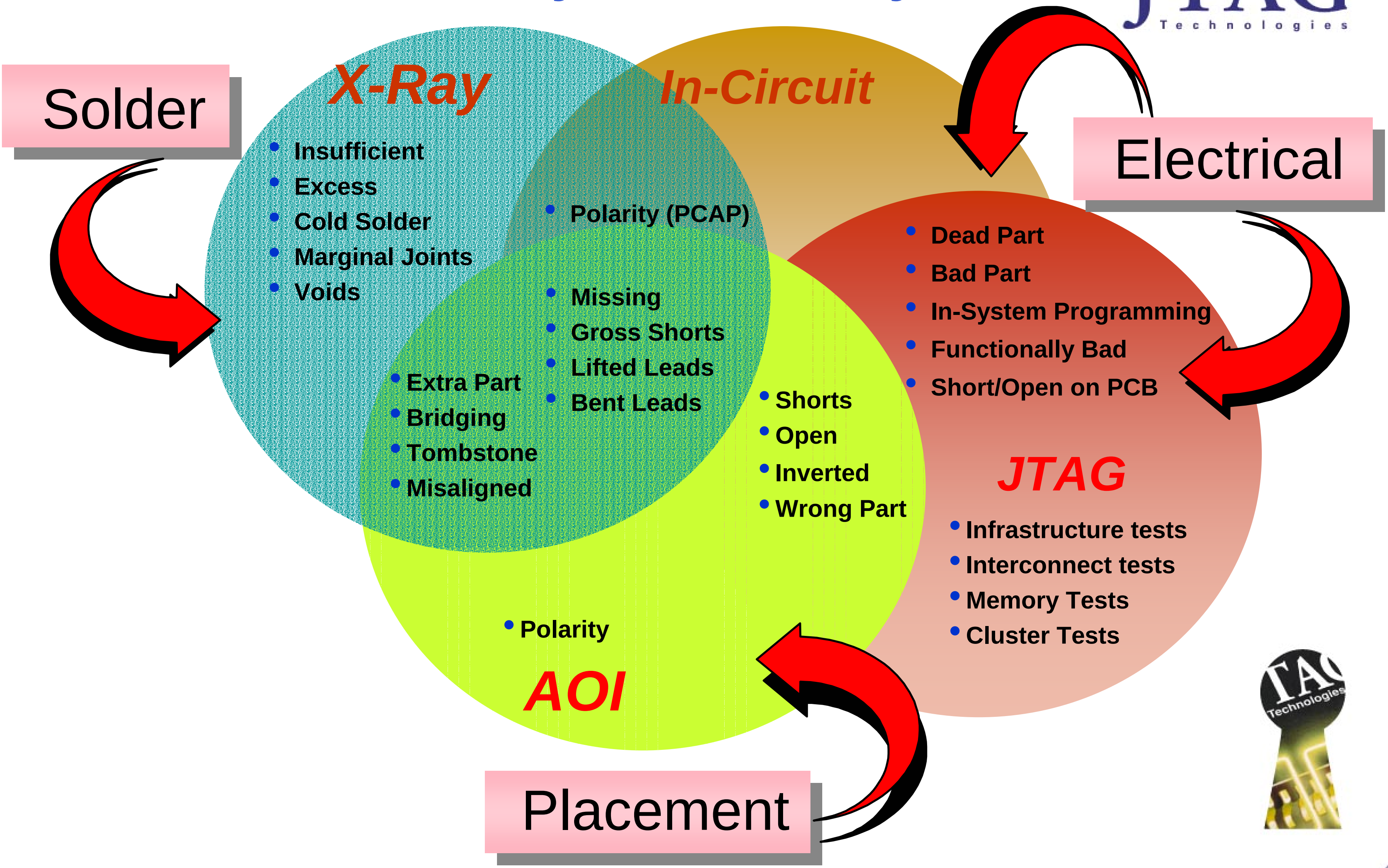
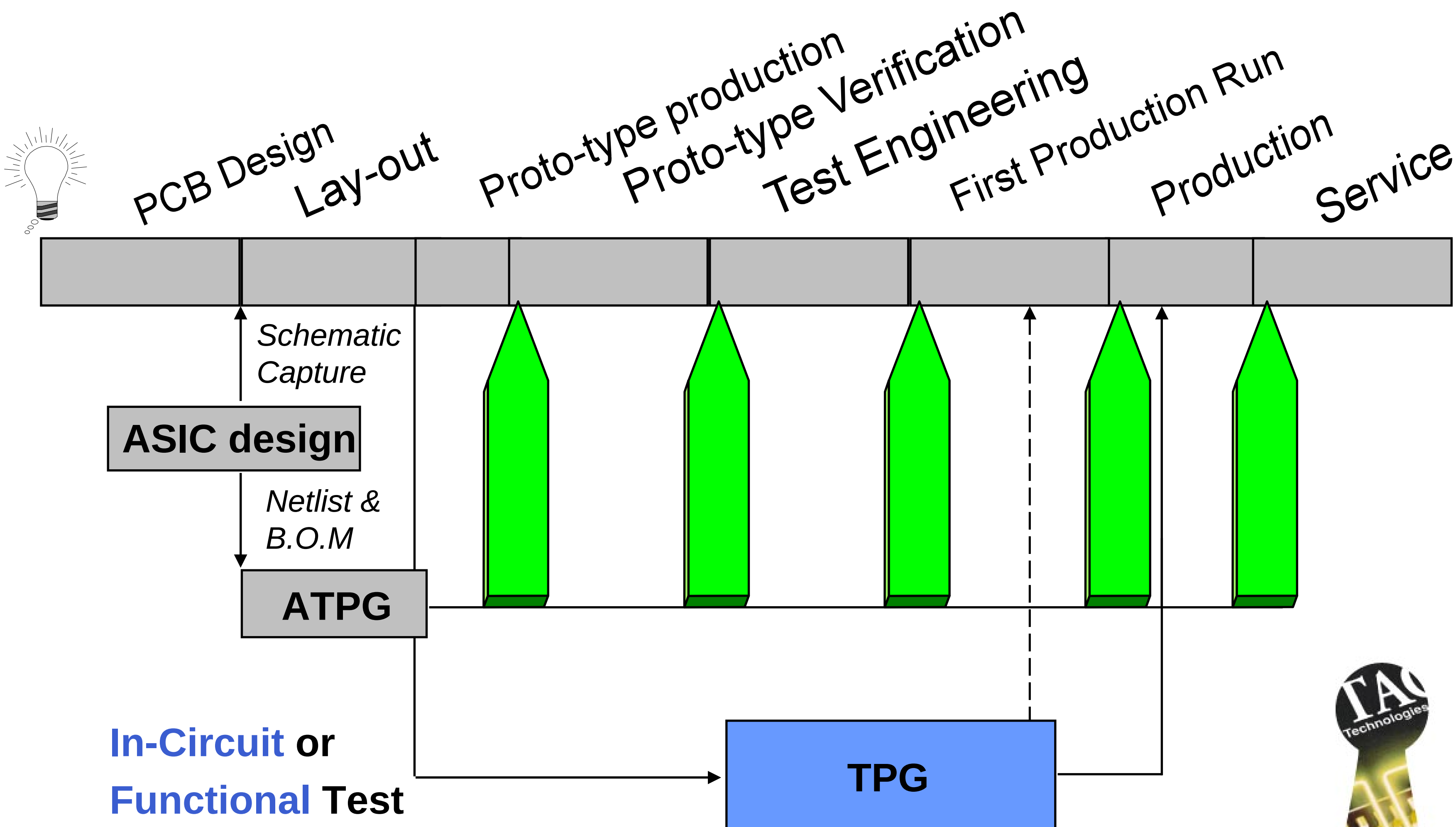
BOUNDARY-SCAN DFT PRINCIPLES

Getting the maximum test coverage from your Boundary-Scan Chains

ICT, AOI, X-Ray & Boundary-scan



PCB Product Life Cycle



The EXTEST Command Principle

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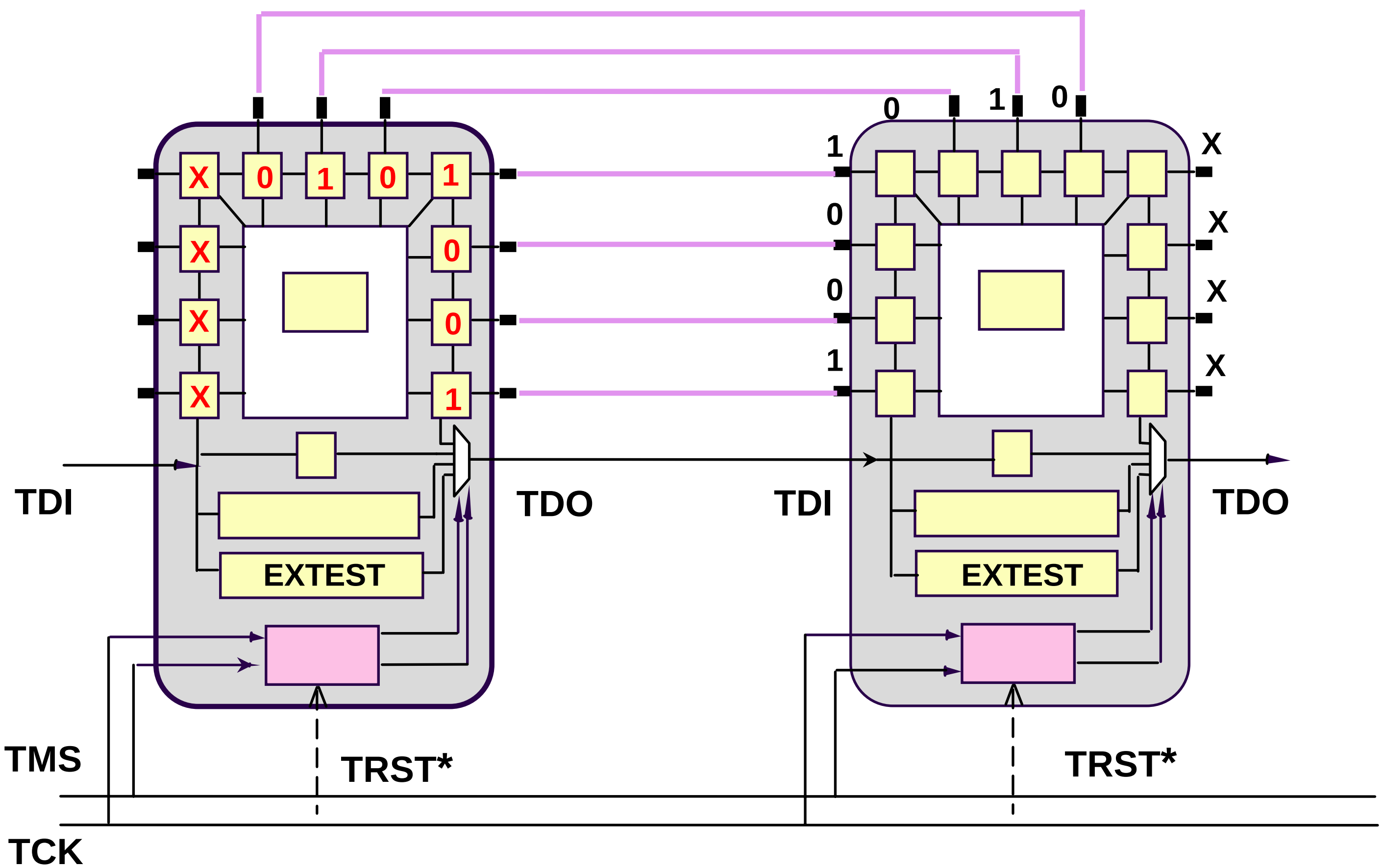
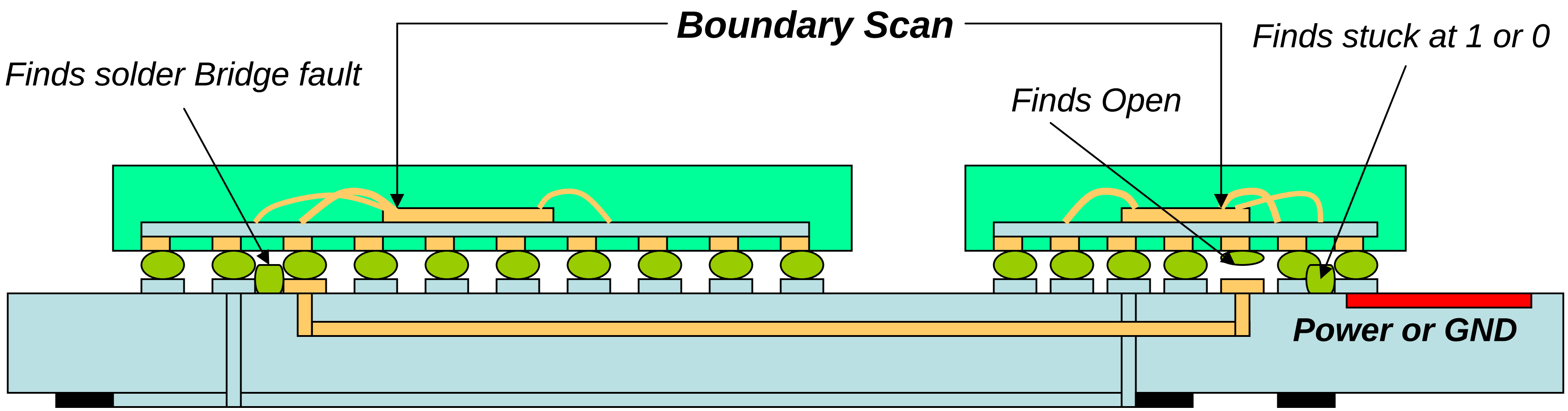


Data Register Shift Output after Update and Capture phases :-
TDI =>XXXX0101001 1001010XXXX=> TDO

Boundary Scan Fault Coverage

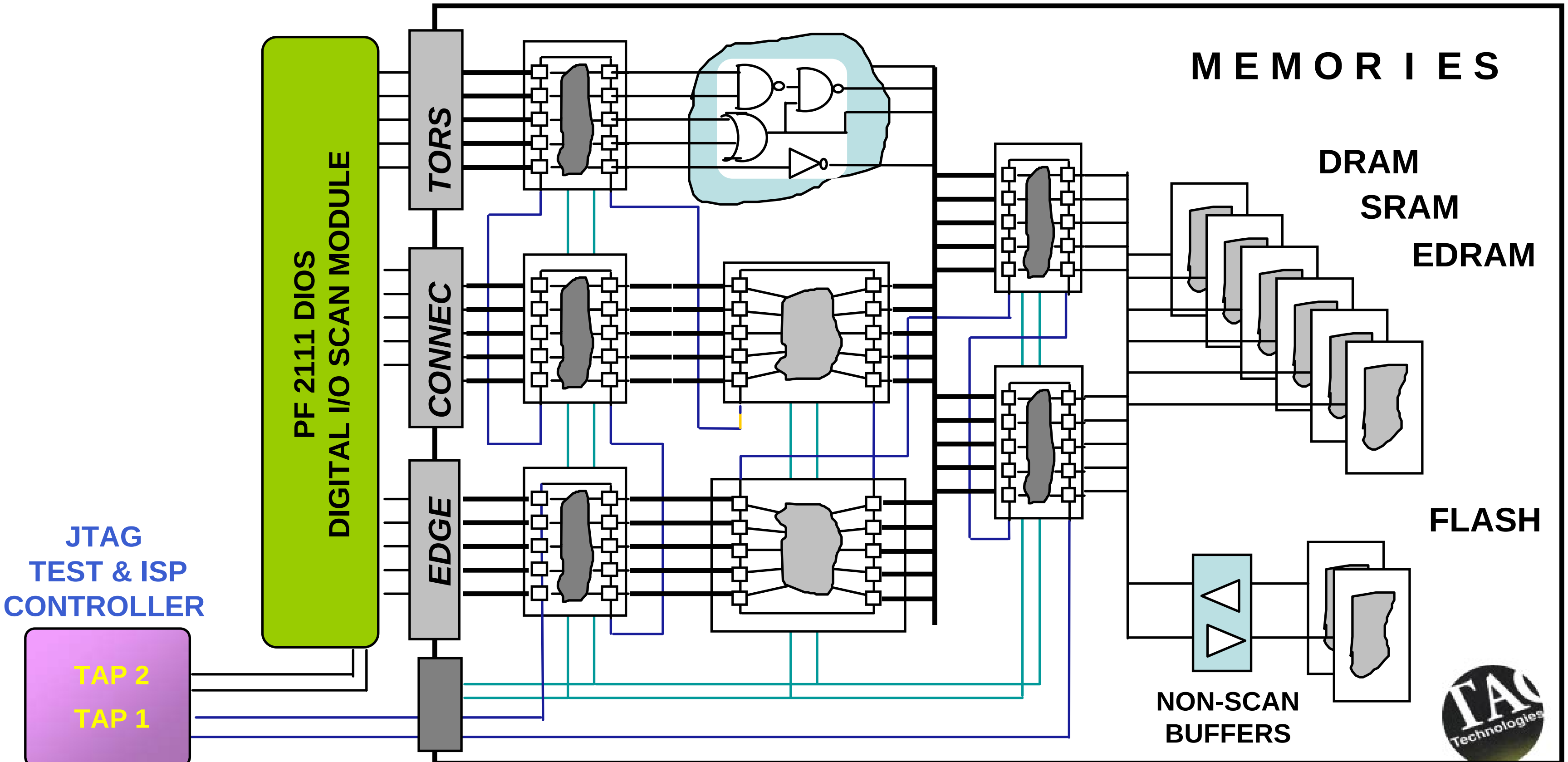


Boundary Scan EXTEST mode – Connectivity path tested:

> **scan cell (driver) > bond wire > leg > solder > interconnect (board trace) > solder > bond wire > scan cell (sensor)**

ESD damaged Boundary-Scan Cells will be found

Boundary-Scan Implementation At PCB Level



Basic DFT Concepts

- **Involve the Test Engineer early in the design process**
- **Choose components carefully**
- **Provide TAP connector(s) or other means of access to the TAP signals. Don't forget easy access to PWR/GND**
- **Consider using multiple chains (no loss of test coverage)**
- **Scan signal terminations -- Pull-ups, buffers, TCK termination**

Basic DFT Concepts

Design For Test - Component Selection

Where possible ensure that device silicon has been verified against latest BSDL file –some IC vendors state this within BSDL file header.

Select IEEE 1149.1 compliant devices where possible –take note of any attribute compliance conformance / warning statement in the BSDL file.

```
--------------------------------------------------BSDL-------------------------------------------------------
        --      Package      : 240-Pin Power Quad Flat Pack
        --      BSDL Version  : 3.00
        --      BSDL Status   : Tested
-- Verification  : Complete IEEE 1149.1 device implementation tested
 --             against BSDL file by JTAG Technologies
-----------------------------------------------------------------------------------------------------------
attribute COMPLIANCE_PATTERNS of isp2032V: entity is "(RESET, ispEN) (10)";
```

Basic DFT Concepts

- Control of non-boundary-scannable devices - Determine how they effect test coverage and provide control from scannable pins (reset, OE, etc.)
- Consider cluster tests and use of DIOS modules
- Flash programming - Verify scan access to all address / data / VPP /control pins, route WE to TAP connector (not required, but will speed up programming)
- BSDL files
  - Check syntax
  - Look for special compliance requirements
  - Check for post-configuration issues

JTAG Technologies

Design For Test - Component Selection

- Select IEEE 1149.1 compliant devices where possible – take note of any attribute compliance conformance / warning statement in the BSDL file.

- Try and avoid devices that use dual-purpose boundary-scan TAP pins that require control of additional JTAG Enable pin.

JTAG Technologies

Design For Test - Component Selection

- **All 1149.1 compliant devices must support the mandatory instruction set of *BYPASS, SAMPLE/PRELOAD, EXTEST,* and it is highly desirable if the optional instructions *HIGHZ* and *IDCODE* are supported.**

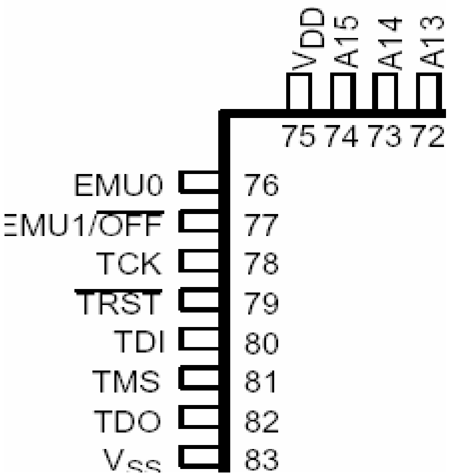
- **Where possible select programmable logic devices that are IEEE 1532 compliant (support of concurrent programming).**

- **Designers are responsible for the level of DFM and DFT implemented within board designs – put pressure on IC vendors to provide a high level of 1149.1 compliance.**
  If NOT use alternative suppliers !

Design For Test
Component Selection

Compatible vs Compliant

•**IEEE-1149.1†-Compatible Scan-Based Emulation**



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TMS320C203 devices incorporate scan-based emulation logic for code-and hardware-development support. Scan-based emulation allows the emulator to control the processor in the system without the use of intrusive cables to the full pinout of the device. The scan-based emulator communicates with the ’C203 by way of the IEEE 1149.1 (JTAG) interface. Note: The TMS320C203, like other DSPs in the TMS320C20x/TMS320C24x families, ***does not include boundary scan***. The scan chain of ’C203 device is useful for emulation functions only.

Design For Test - Scan Chain Partitioning

➢ **TDI and TDO are used to daisy chain devices into a single scan chain, unless:**

- **Devices must be contained within a separate chain to be compliant with other third-party debuggers or emulators e.g. DSP's.**
- **CPLD's may require separate chains for their associated configuration software. This is not a problem if devices are IEEE 1532 compliant.**
- **It may be easier to segment different logic/voltage families e.g. ECL / TTL or 1.8V, 2.5V and 3.3V by using different chains.**
- **It may be better to partition designs into functional blocks for improved diagnostic resolution, and optimized test vector execution.**

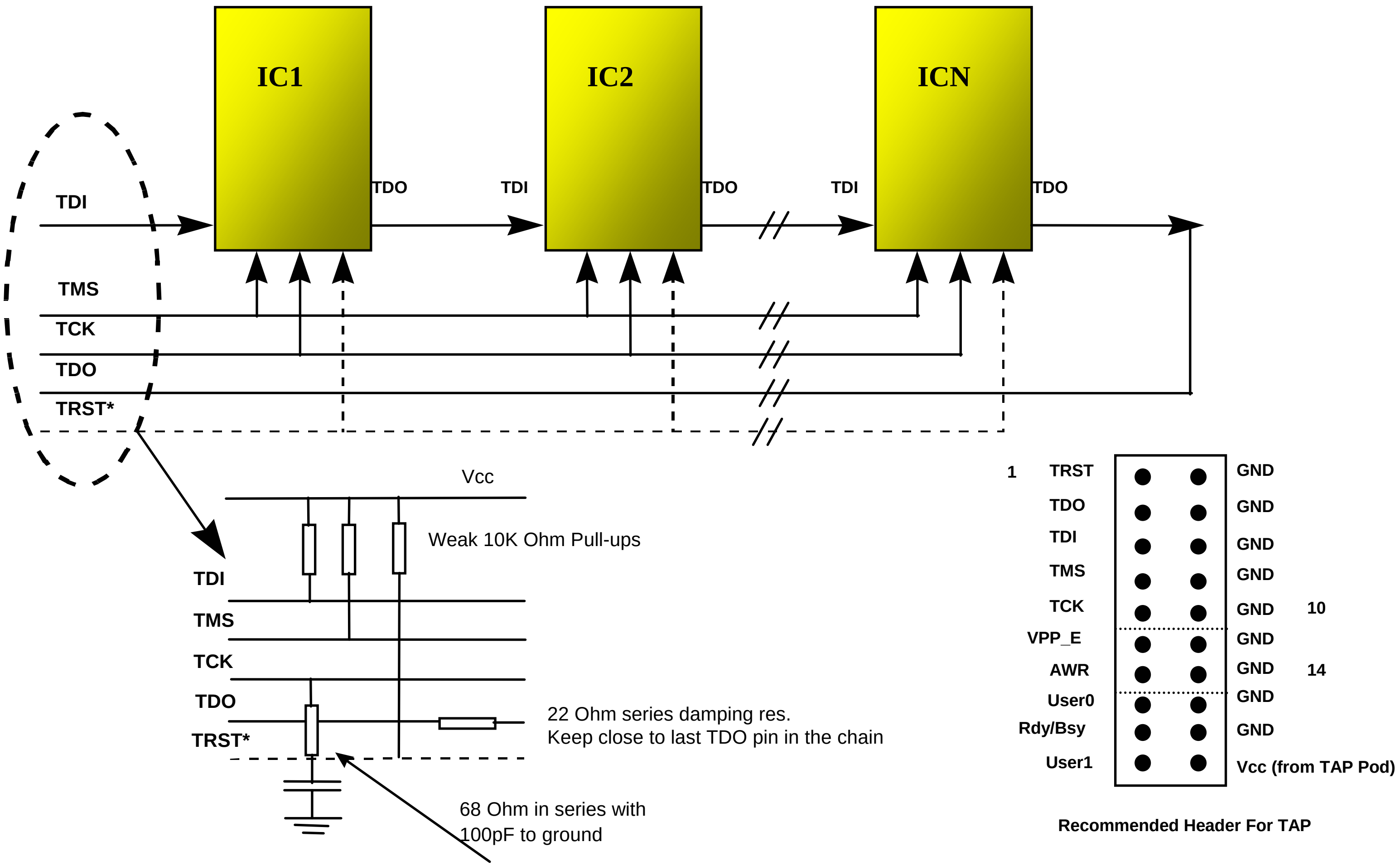
Design For Test - Scan Chain Partitioning

➢ **Where possible ensure all boundary-scan TAP signals are accessed via primary board edge connector. This eliminates the need for bed-of-nails probing.**

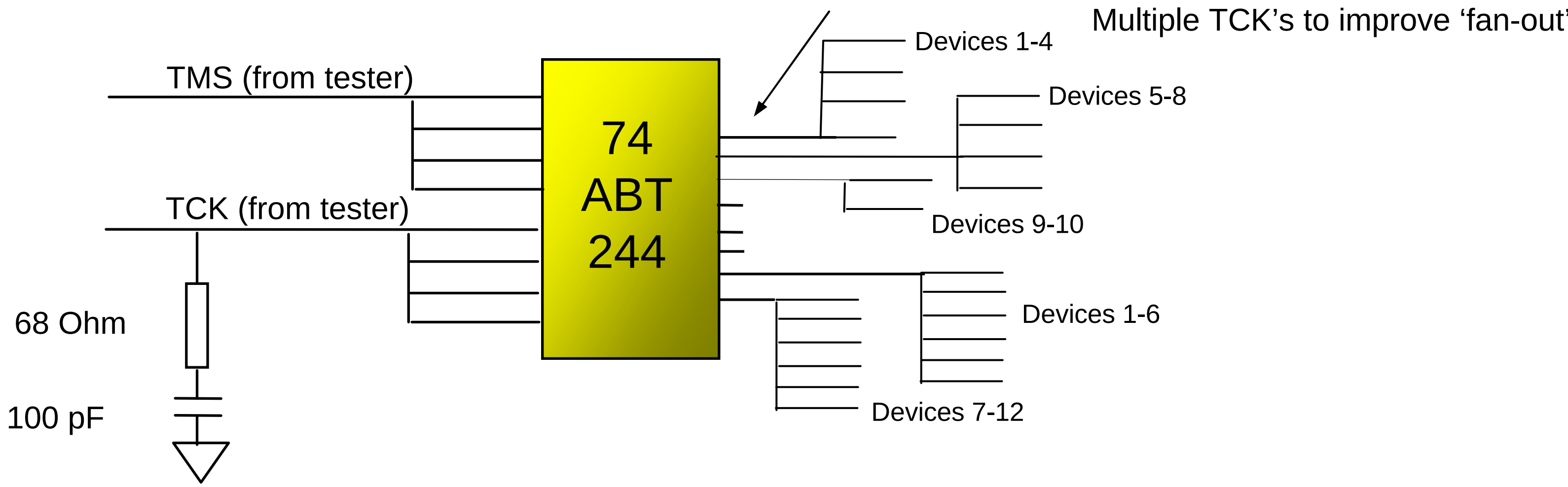
➢ **Keep boundary-scan signal paths as short as possible, avoid unnecessary trace looping – specify the routing of the TCK and TMS signals as CRITICAL.**

➢ **It is good design practice to buffer all 1149.1 signals interfacing to the board to ensure signal integrity; particularly TCK and TMS.**

Design For Test - Scan Chain Layout



Buffer Broadcast Control Signals TMS,TCK, (TRST)



- **Board fan-out of control lines TMS and TCK must also be considered**
  - **A general rule of thumb is if track lengths are fairly short – fan out to 4 to 6 devices from buffered output is acceptable (TCK is more critical than TMS)**
- **If track lengths are fairly long it may be worth considering a fan-out of 1 or 2.**
- **These guidelines may be considered over cautious but it may be the difference between a design functioning reliably or not at all.**

Note: In some circumstances TRST can also require buffering however this is not usually a requirement since rarely all IC's feature this signal.

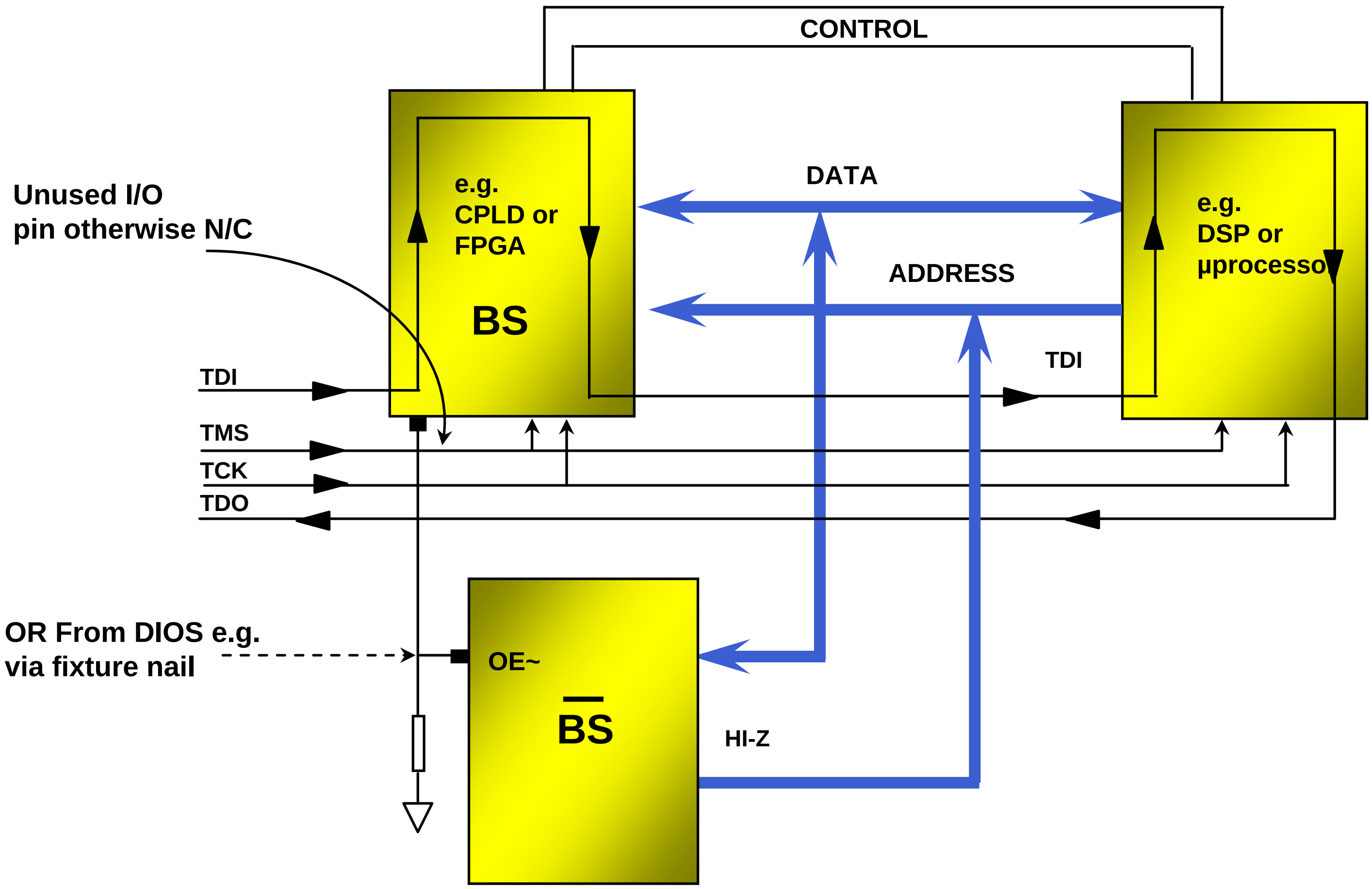
TRST Termination Considerations

- Improper termination of TRST signal can cause board to power up in an unsafe state. Here are two options for dealing with this:

  1. Use a Power-up reset circuit to apply 5 five TCK pulses while holding TMS high (preferred).

  2. Tie TRST low with a resistor of appropriate value.

Utilize Unused I/O pins As Test Nets

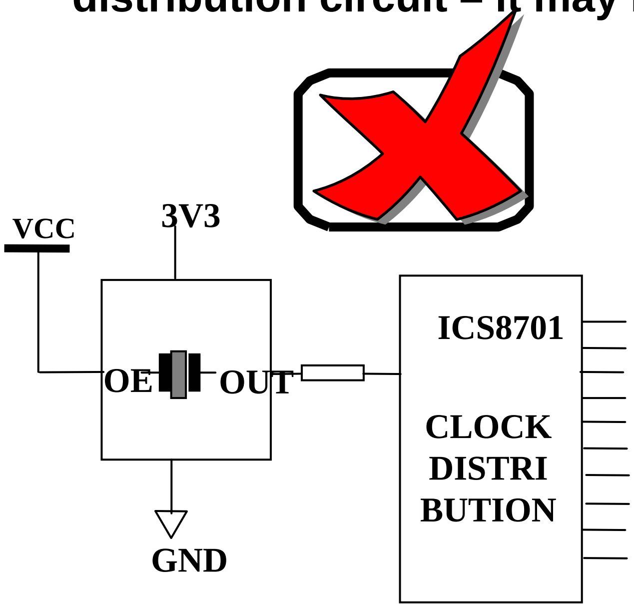


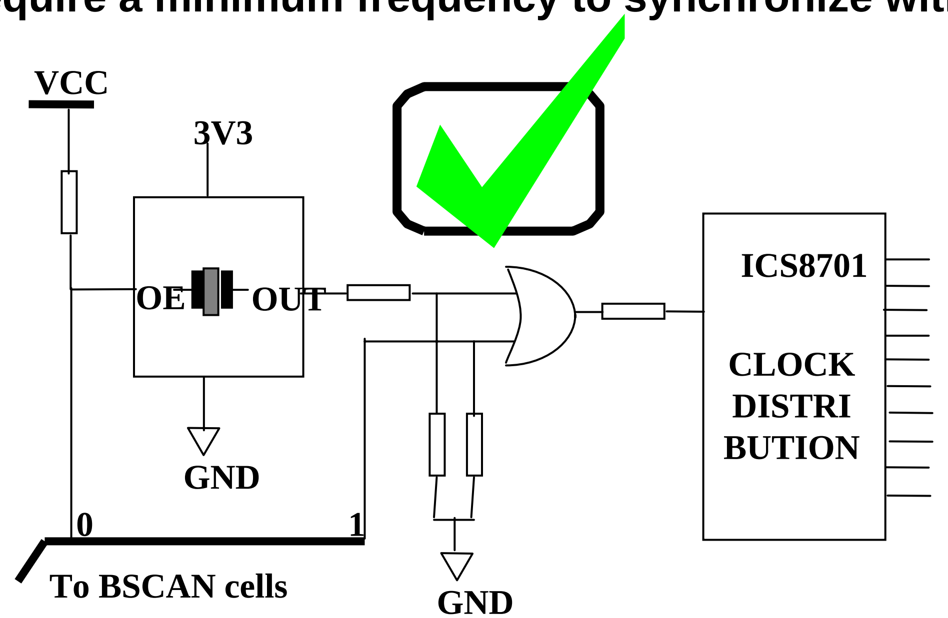
Don't forget to include a way to disable Watchdog timers!

Design-for-Test - Clock Signals

JTAG In-Circuit Requirements

- Ensure where on-board clocks interfere with boundary-scan testing – these clocks can be disabled via boundary-scan cells.
- Where a clock is required to control devices for boundary-scan testing e.g. synchronous DRAM – provide the capability for replacing on-board clock with a test clock via boundary-scan cell.
- When using this technique, check on minimum operation frequency of clock distribution circuit – it may require a minimum frequency to synchronize with PLL.





Design-for-Test - Physical Bypassing

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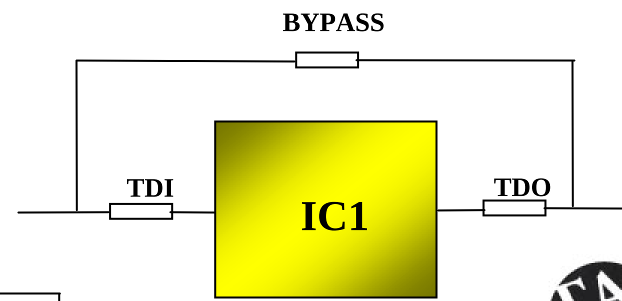
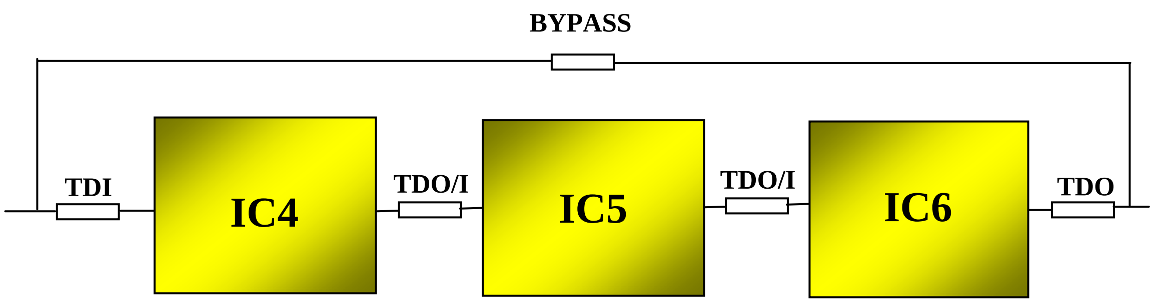
JTAG In-Circuit Requirements

- **Consider Bypass resistors.**
  1. **Unknown parts.**
  2. **Unreleased Silicon**
  3. **Extra testpoint**
- **When Bypassing devices remove resistors TDI and TDO and place resistor BYPASS**
- **TDI must be removed to prevent IC1 from receiving an erroneous instruction which may cause unpredictable states, and TDO must be removed to prevent contention.**

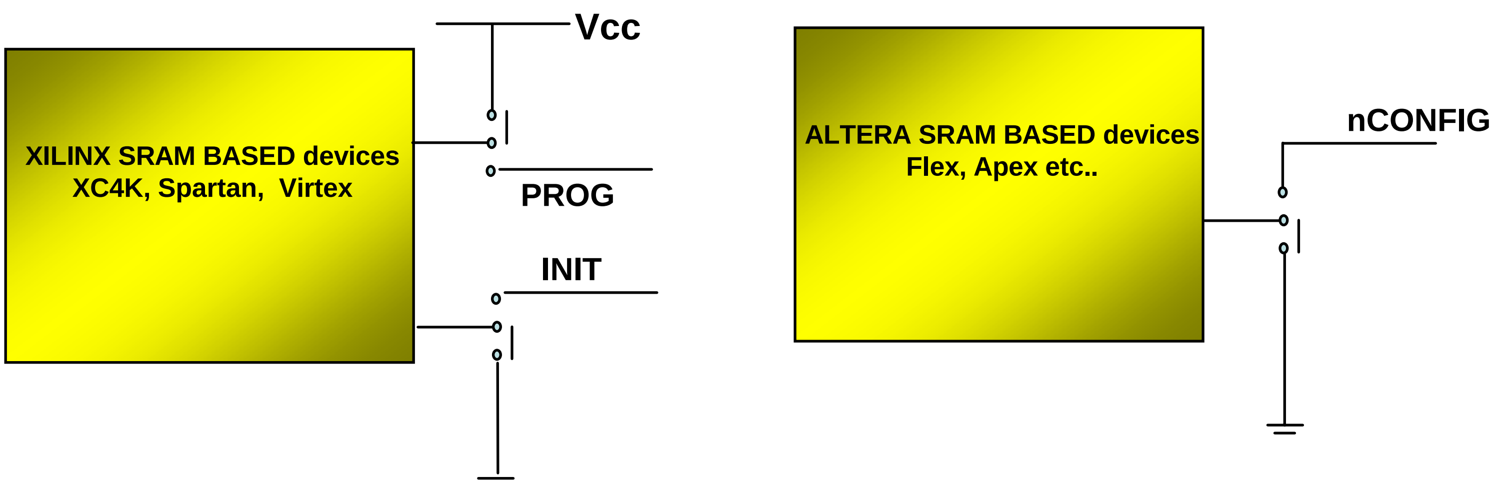
Single device



Multiple devices

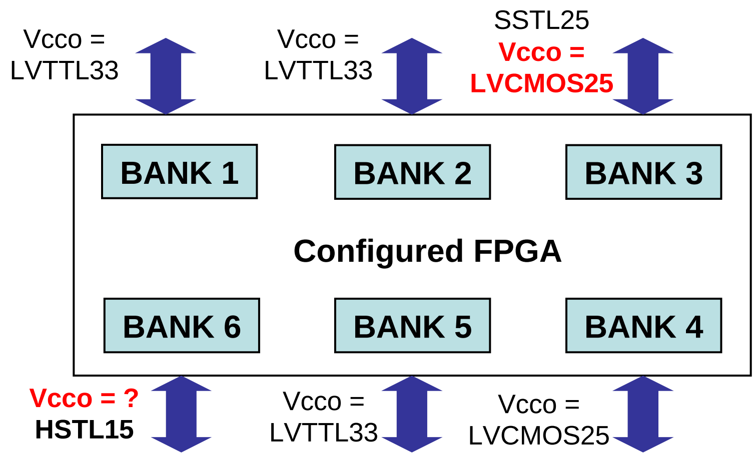


Special Considerations for SRAM FPGA's



- SRAM based FPGA's are often subject to changes in their BSCAN behaviour (capability) at different stages during their configuration / programming sequence - read application notes carefully for full details.
- Hold off configuration.
- A low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

FPGA Re-configurable I/O Considerations
(Programmable voltage levels)



- **In the pre-configured state I/O pins will default to LVTTL33 or default voltage wired to Vcco.**
- **This can cause problems where IO pins can be driven to the default Vcco voltage ? (Bank 6) and the configured output standard HSTL state of 1.5V, the un-configured default Vcco state will be 3.3V – this could damage HSTL15 devices connected to this bank.**
- **In these circumstances it is advisable to configure FPGA devices prior to conducting boundary-scan interconnect tests or ensure Vcco is hard-wired to the configured voltage level.**

FPGA Re-configurable I/O Considerations
(Programmable Driver/Receivers)

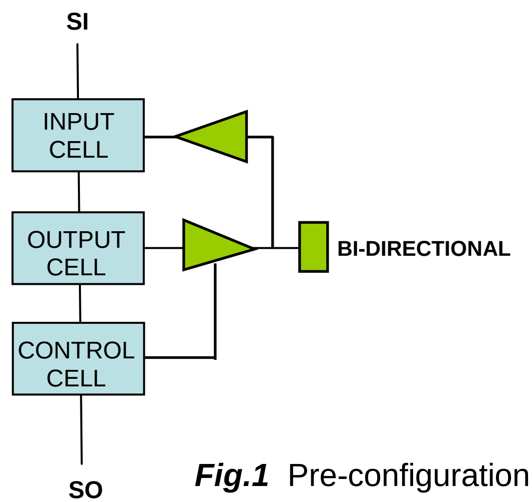


Fig.1 Pre-configuration

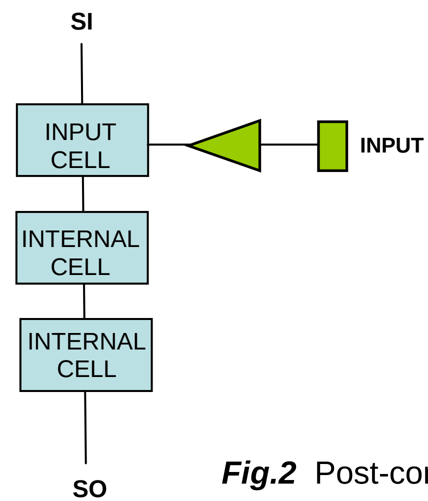


Fig.2 Post-configuration

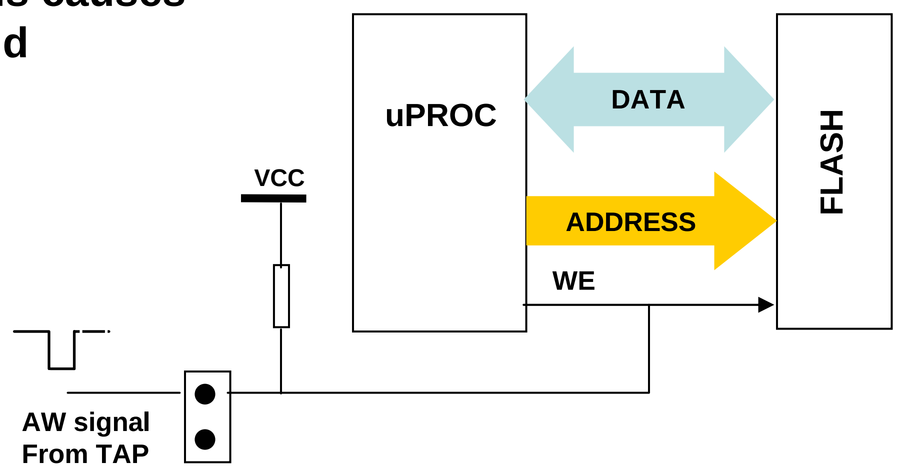
- **In the pre-configured state I/O's are defined as bi-directional cells, which is how the operation is specified in the pre-configured BSDL file description.**
- **Once the device has been configured the boundary-scan cells on each of the signal pins may change as shown in *Fig.2***
- **In this case boundary-scan tests will need a *post-configured* BSDL file.**

Note: The Xilinx FPGA design environment provide the option to export post-configuration BSDL files.

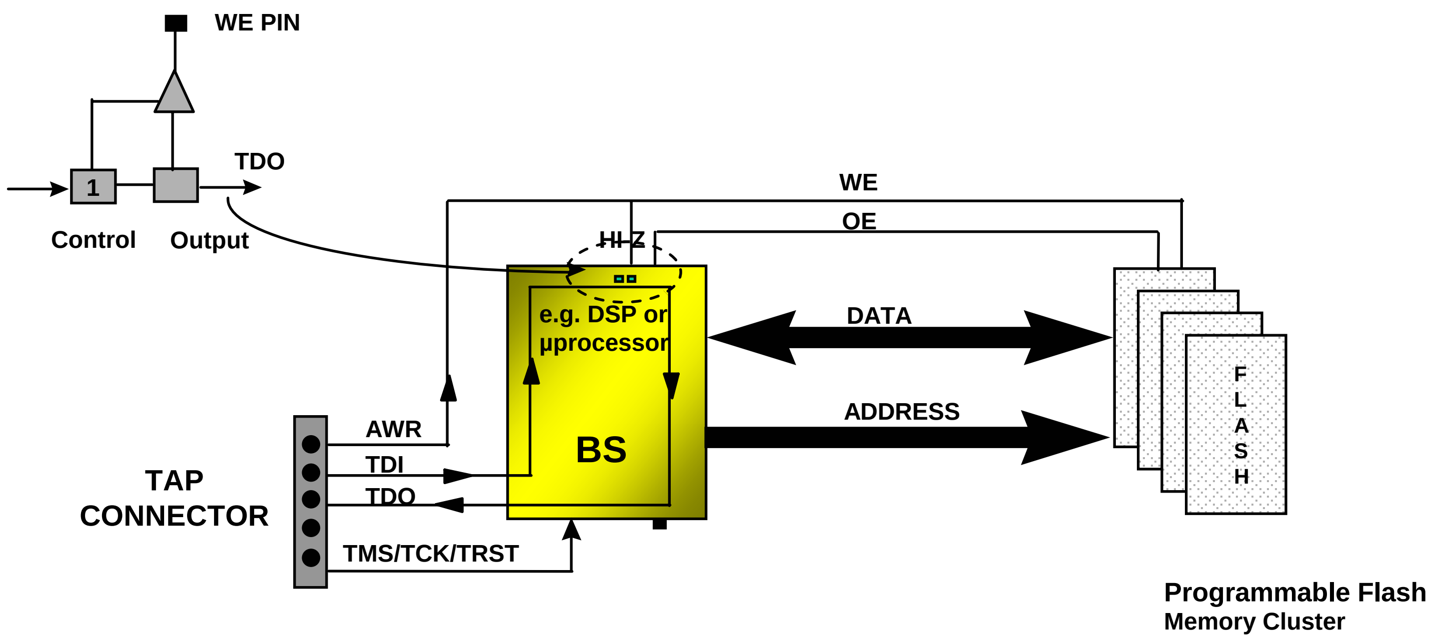
Design-for-Test - AutoWrite^{TM} Access

JTAG Flash Programming Requirements

- In order to optimize the flash programming sequence connect flash memory WE signal to the AutoWrite^{TM} JTAG controller signal pin.
- Ensure that the WE signal is pulled high (1K) on the board – this will ensure that the AW signal driven by the JTAG controller de-asserts to a logic high state
- Ensure shortest possible chain length for flash memory access – if this is NOT possible ensure devices in chain can be placed in BYPASS or preferably HIGHZ – this will prevent any bus contention issues.
- Ensure that when devices are placed in HIGHZ, the high impedance state of the outputs does not affect the internal functionality of the board If this causes a problem, these signals should be terminated to a safe state.



Connect WE_ to AutoWrite Input for Optimized Flash Programming Performance




```
"125 (BC_2  ,  we0_b_bs,  output2  ,   X),"  &
:
"143 (BC_4  ,  wr_b,   input    ,   X),"  &
"144 (BC_2  ,  wr_b,   output3  ,  0,    145,   1,   Z)," &
"145 (BC_2  ,  *,        controlr ,  1),"  &
```

Design For Test – Control Cells

Ganged control cells may lead to problems.

```
*CHAIN CELL PORT CELL SAFE CONTROL DISABLE DISABLE *
* POS TYPE NAME FUNCTION VALUE CELL VALUE RESULT *
*************************************************************************
*************************************
“74 ( BC_2, * , controlr , 1), “ &
“73 ( BC_1, WE , output3 , 0 , 74, 1, Z), “ &
“72 ( BC_1, OE , output3 , 0 , 74, 1, Z), “ &
“71 ( BC_1, nSDRAS , output3 , 0 , 74, 1, Z), “ &
“70 ( BC_1, nSDCAS , output3 , 0 , 74, 1, Z), “ &

“53 ( BC_1, A25 , output3 , 0 , 74, 1, Z), “ &
“52 ( BC_1, A24 , output3 , 0 , 74, 1, Z), “ &
“51 ( BC_1, A23 , output3 , 0 , 74, 1, Z), “ &
“50 ( BC_1, A22 , output3 , 0 , 74, 1, Z), “ &
“49 ( BC_1, A21 , output3 , 0 , 74, 1, Z), “ &
“48 ( BC_1, A20 , output3 , 0 , 74, 1, Z), “ &
“47 ( BC_1, A19 , output3 , 0 , 74, 1, Z), “ &
BSDL
```

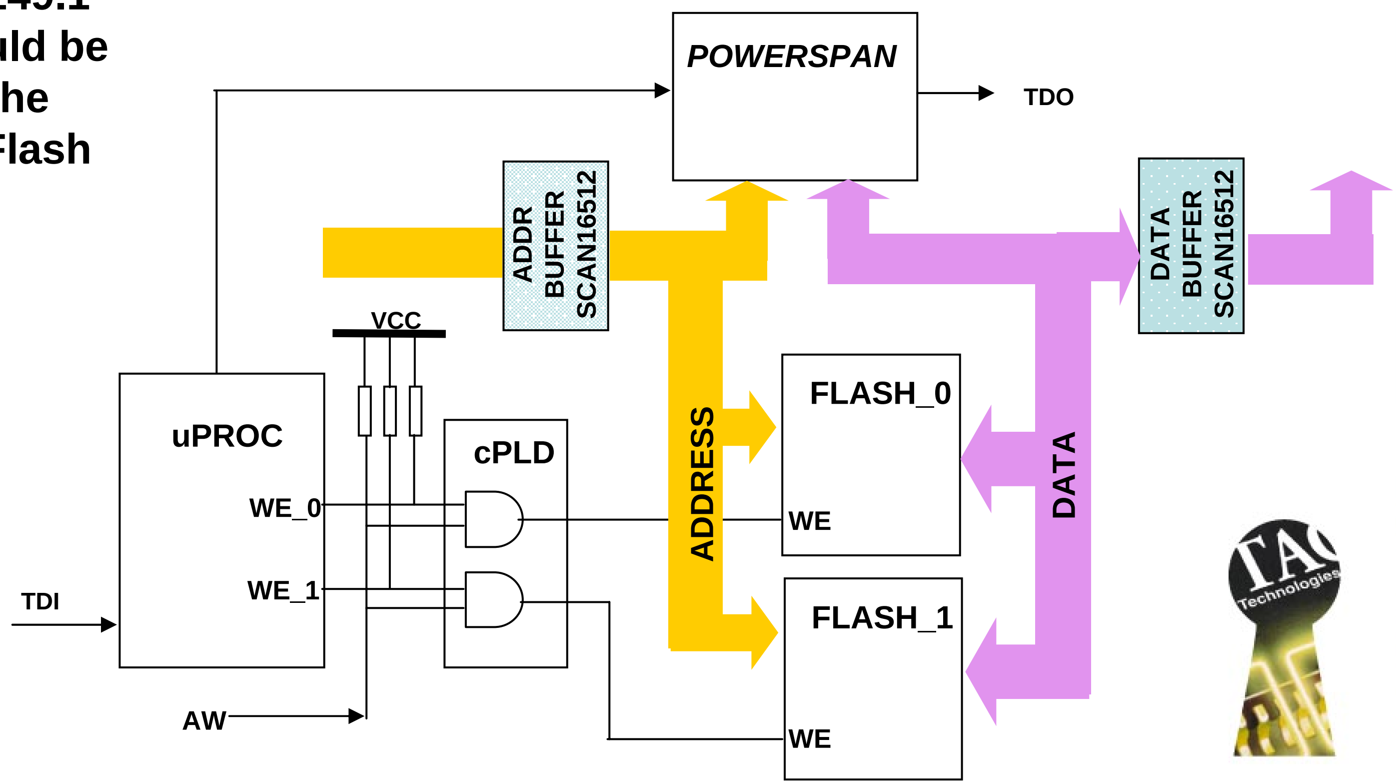
Design-for-Test - AutoWrite™ Access

JTAG Technologies

Overcoming tri-state limitations

- **Utilizing AW signal when device driving WE signal is a 2-state signal can cause bus contention – Gate with Glue logic or PLD in bypass.**

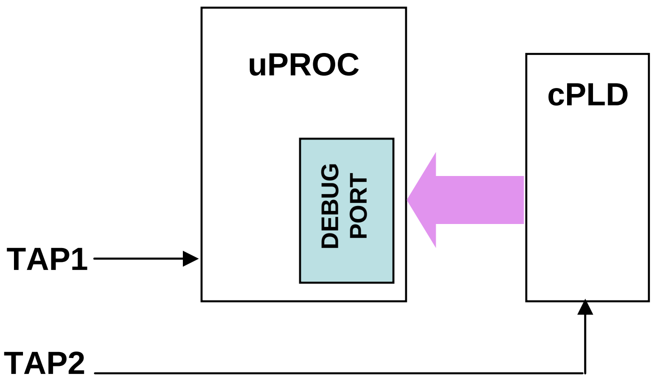
Alternatively a 1149.1 buffer device could be placed between the uPROC and the Flash memory.



Design-for-Test - Ensuring Correct Power-up Status

JTAG – Device Specific DFT Requirements

- Some boundary-scan devices require special consideration in order to select between the debug (default) and JTAG mode of operation.
- The devices will default to the debug mode on power-up unless certain bits in the device Configuration Register are set to a logic “0” and“1” respectively.
- This can be resolved by configuring the debug port pin status within a PLD or via a buffer, to set the relevant data lines to the required state following HRESET.
- If this functionality is embedded within a PLD, it will have to be placed in a separate chain so that it can be in-system configured and subsequently placed in BYPASS mode to provide the correct debug port pin status on power-up.



Other DFT Considerations

- **Schematic Capture - Give every digital net a meaningful name**
  - **Development tools are net based**
  - **Diagnostics use net names from netlist**
  - **Use separate symbols for each section of multichip modules**

- **ASIC Design – Think from the test point of view**
  - **Boundary register cells should be I/O cells whenever possible**
  - **Use individual control cells for each boundary register I/O cell**

- **Verify BSDL file!!**

Boundary-Scan Coverage Report

```
DESIGN  : jt2153
TOOL    : BFCE Version 2.1
OPTIONS : -p50
```

NET NAME:	Bi	Bo	Bio	Btst	Bpwr	Pi	Po	Pio	Ci	Co	Cio	pins	weight	pins tested	net tested	net maxim	remarks
3V3	0	0	0	0	8	0	0	0	0	0	26	34	0.0	0.0	0%	0%	I V
5V	0	0	0	0	8	0	0	0	0	0	63	71	0.0	0.0	0%	0%	I V
$1I295\CC403	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
$1I296\$1N456	0	0	0	0	0	0	0	0	0	0	4	4	1.0	2.0	50%	50%	W
$1I296\$1N464	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
$1I296\$1N473	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
$1I296\$1N474	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
$1I296\$1N503	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
CC400	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC401	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC402	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC408	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC409	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC412	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC413	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC416	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
CC417	0	0	0	0	0	0	0	0	0	0	3	3	0.0	0.0	0%	0%	
DIG_RH	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
DIG_RL	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
GND	0	0	4	0	24	0	0	0	0	0	108	136	0.0	0.0	0%	0%	I V
GOE	4	0	0	0	0	0	0	0	0	0	1	5	0.0	0.0	0%	60%	P
INC_RH	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV406	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV407	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV410	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV411	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV414	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV415	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV418	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	
VV419	0	0	0	0	0	0	0	0	0	0	2	2	0.0	0.0	0%	0%	

Boundary-Scan Coverage Report

JTAG Technologies

```
DESIGN : jt2153
TOOL   : BFCE 2.5 - 20030602
OPTIONS: -h -nd
```

NET	PART	PIN	TYPE	DRIVEN ACTUAL	SENSED ACTUAL	DRIVEN MAXIMAL	SENSED MAXIMAL
D1R	R600	6	Cio	B	B	B	B
	V600	2	Co	B	-	B	-
D2	R602	5	Cio	B	-	B	-
	D600	68	Bio	B	B	B	B
D2R	R602	6	Cio	B	B	B	B
	V600	6	Co	B	-	B	-
D3	R604	6	Cio	B	-	B	-
	D600	79	Bio	B	B	B	B
D3R	R604	5	Cio	B	B	B	B
	V600	11	Co	B	-	B	-
D4	R606	6	Cio	B	-	B	-
	D600	7	Bio	B	B	B	B
D4R	R606	5	Cio	B	B	B	B
	V600	15	Co	B	-	B	-
DATA0	D600	40	Bio	B	B	B	B
	D301	21	Cio	B	B	B	B
	D300	21	Cio	B	B	B	B
	D201	2	Bio	B	B	B	B
DATA1	D600	41	Bio	B	B	B	B
	D301	22	Cio	B	B	B	B
	D300	22	Cio	B	B	B	B
	D201	4	Bio	B	B	B	B
DATA2	D600	42	Bio	B	B	B	B
	D301	23	Cio	B	B	B	B

Boundary-Scan Coverage Report

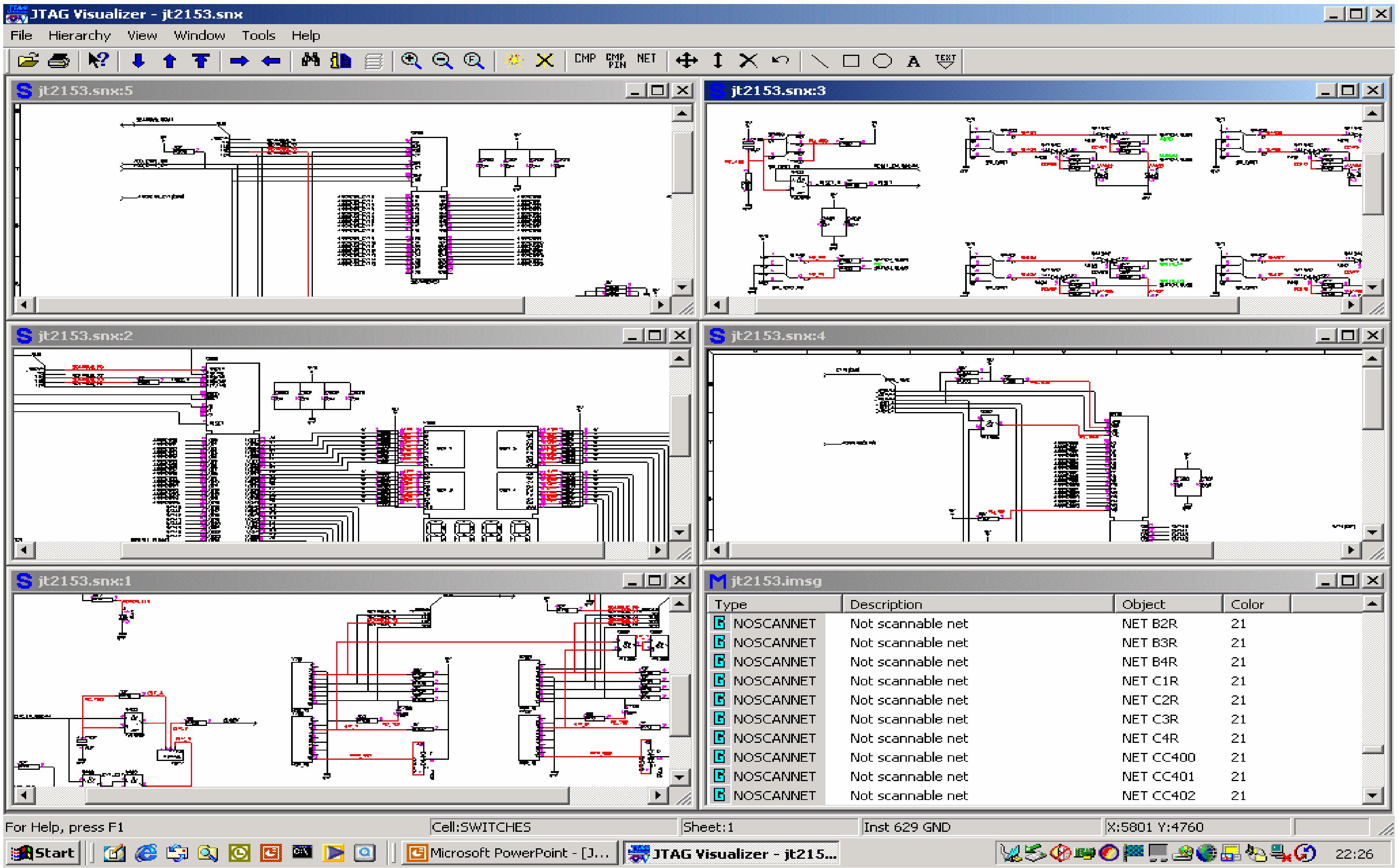
JTAG

PIN STATISTICS:		NET STATISTICS:	
Total number of pins in table	440	Total number of nets in table	84
Total number of pins not in table	463	Total number of nets not in table	178
--		--	
Total number of pins in design	903	Total number of nets in design	262
Pins in table:		**Nets in table:**	
Number of ignored power pins	237	Number of ignored power nets	3
Number of ignored other pins	0	Number of ignored other nets	0
Number of evaluated pins	203	Number of evaluated nets	81
--		--	
Total number of pins in table	440	Total number of nets in table	84
Pins not in table:		**Nets not in table:**	
Number of ignored power pins	0	Number of ignored power nets	0
Number of ignored other pins	2	Number of ignored other nets	0
Number of evaluated pins	461	Number of evaluated nets	178
--		--	
Total number of pins not in table	463	Total number of nets not in table	178

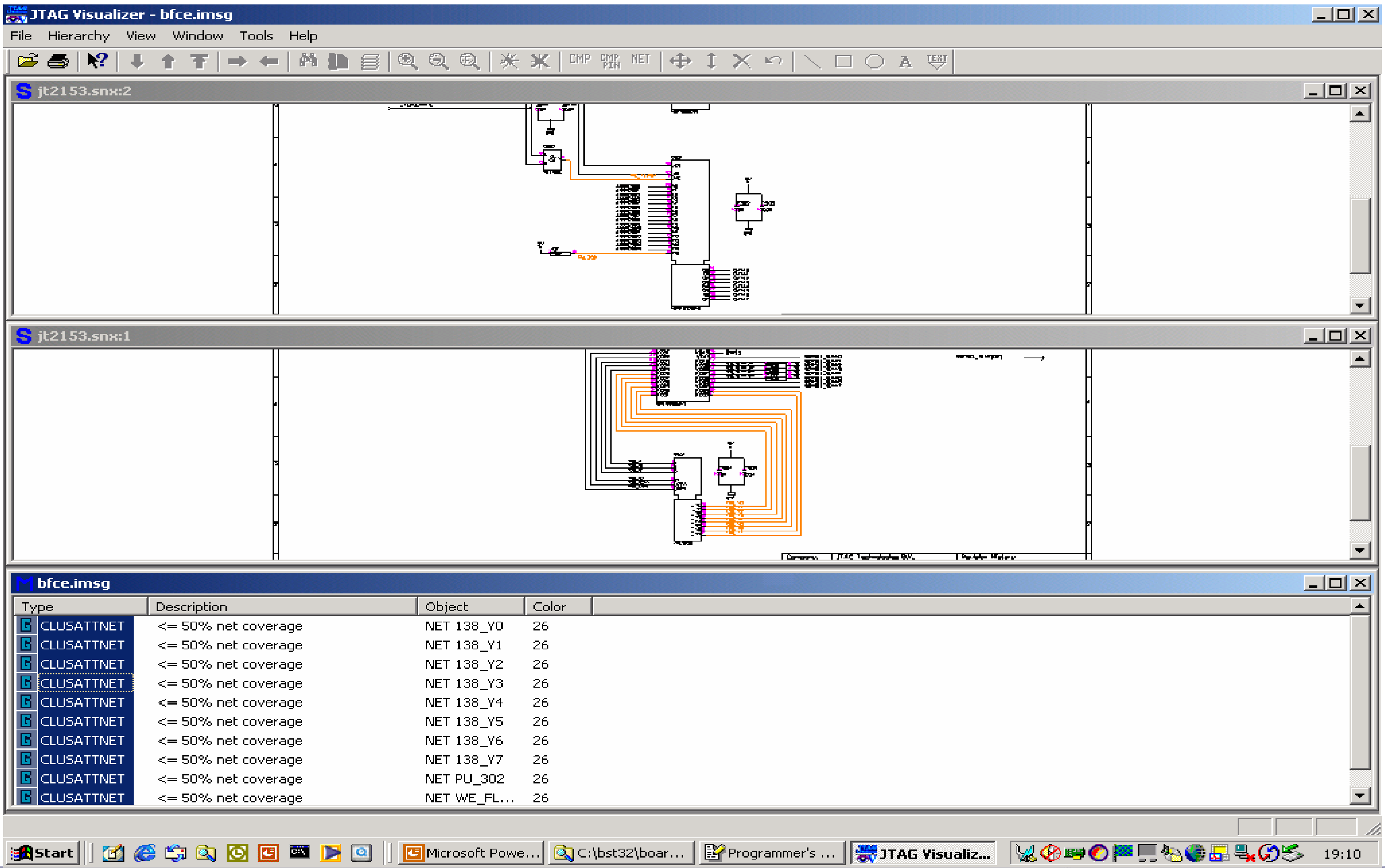
Total number of direct access nets	146
Total number of transp access nets	206
DIRECT BSCAN-ACCESSIBILTY	56%
TRANSPARENT BSCAN-ACCESSIBILTY	79%

Total number of ignored pins	239	Total number of ignored nets	3
Total value of pin coverage	439.5	Total value of net coverage	173.4
Total number of evaluated pins	664	Total number of evaluated nets	259
TOTAL COVERAGE OF EVALUATED PINS	66%	TOTAL COVERAGE OF EVALUATED NETS	67%
Maximal possible pin coverage	489.5	Maximal possible net coverage	190.0
Total number of evaluated pins	664	Total number of evaluated nets	259
MAXIMAL POSSIBLE PIN COVERAGE	74%	**MAXIMAL POSSIBLE NET COVERAGE**	73%

Visualizer: Nets with no scan



Visualizer: Nets with poor scan coverage



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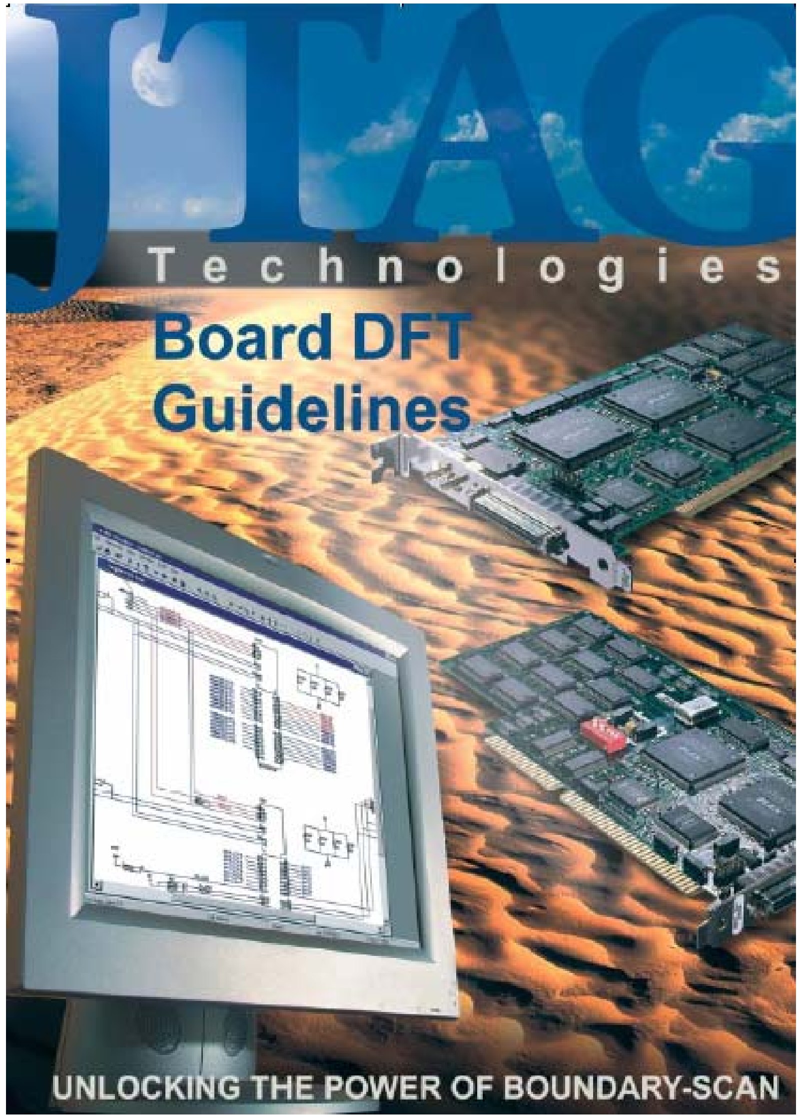

Questions?