

SCHEMATIC REUSE 101 WITH MANAGED HIERARCHY

JOE KWIATEK

ECAD DESIGN/SUPPORT

LUCENT TECHNOLOGIES

BELL LABS ADVANCED TECHNOLOGIES

HOLMDEL DESIGN ENGINEERING SERVICES

jkwiatek@lucent.com



MARLUG - Mid-Atlantic Region Local Users Group
ANNUAL CONFERENCE - OCTOBER 5, 2004
Johns Hopkins University Applied Physics Lab – Laurel, MD

Design Candidates & Considerations

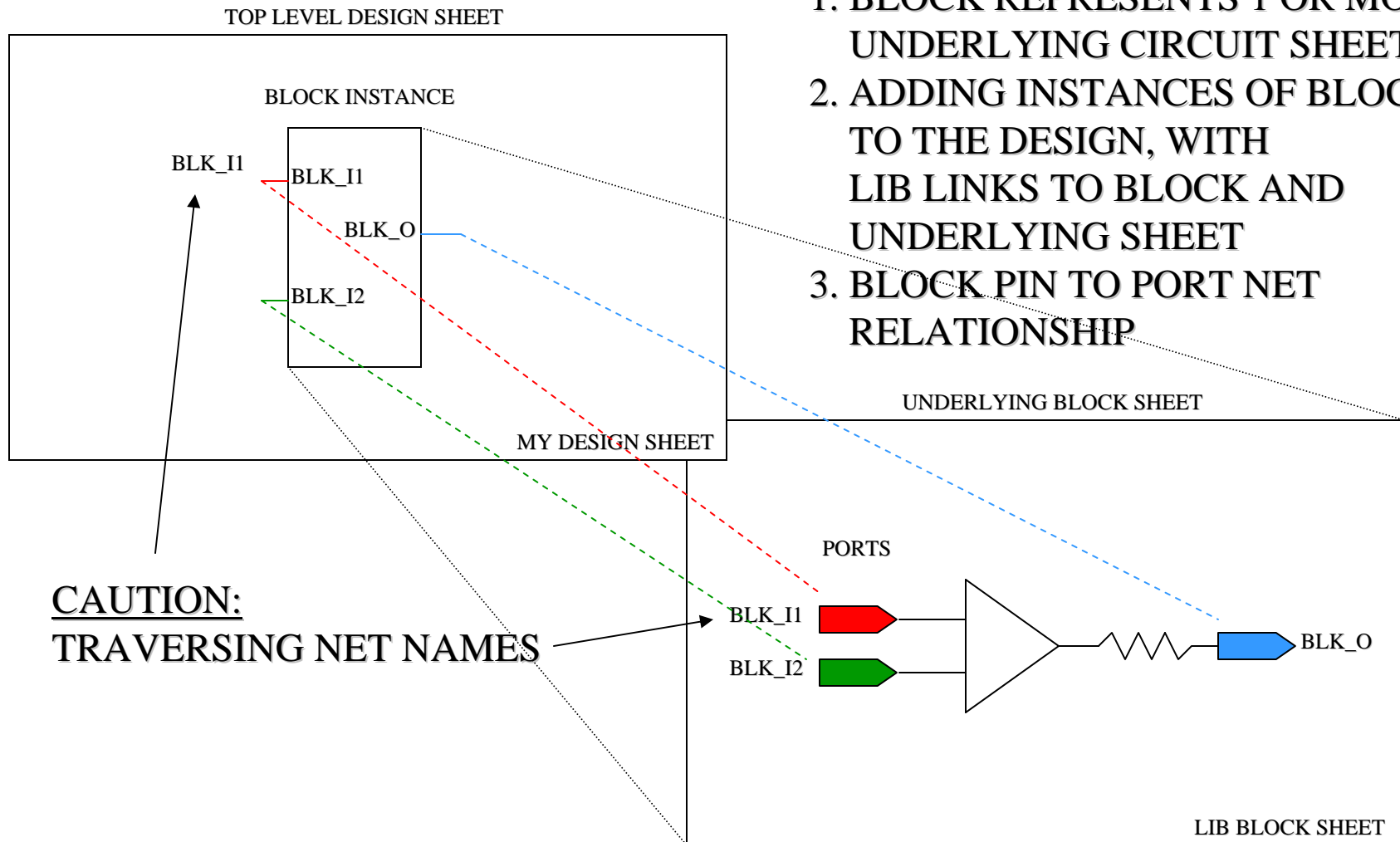


- ✓ **Repeated Sub-circuits.**
 - **Multiple Instances within a Single Design.**
 - **Project: Instances across Multiple Designs.**
 - ✓ **Optical Networking Project**
 - ✓ **Multi PCBs, Repeated Sub-circuits**
 - ✓ **22 Unique Functional Blocks**
 - ✓ **17 Designs**
 - ✓ **Avg 40% Block Usage Per Design**
- ✓ **Community Adapting / Accepting**
 - ✓ **System Architecture - *Modular***
 - ✓ **Circuit Engineering – *Hybrid***
 - ✓ **Sub Circuit Engineer – *Ownership***
 - ✓ **ECAD Design – *Eager, Process***
 - ✓ **Library - *Cooperation***
 - ✓ **Management – *Cost, Interval, Quality***

Hierarchy Basics

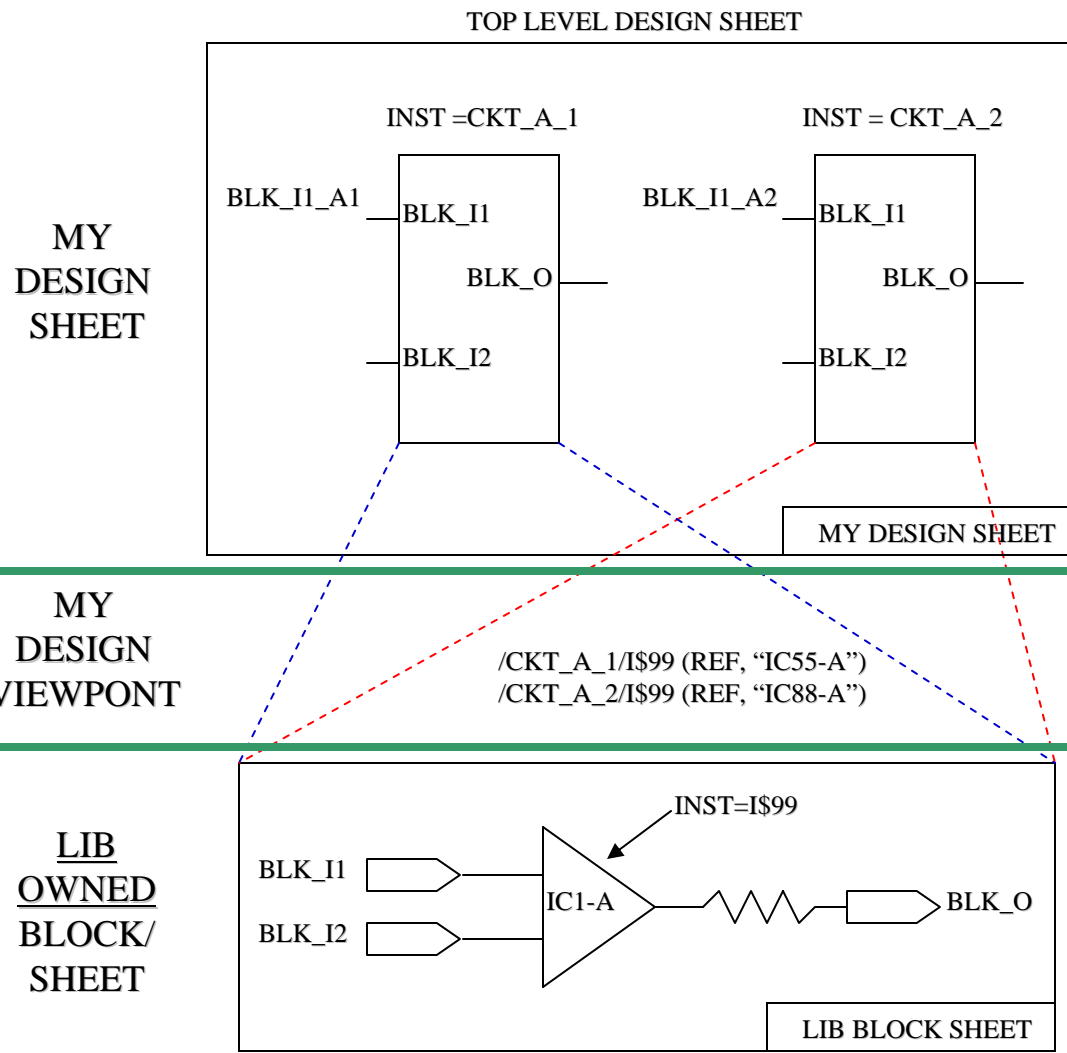
PRIMARY CONCEPTS:

1. BLOCK REPRESENTS 1 OR MORE UNDERLYING CIRCUIT SHEETS.
2. ADDING INSTANCES OF BLOCKS TO THE DESIGN, WITH LIB LINKS TO BLOCK AND UNDERLYING SHEET
3. BLOCK PIN TO PORT NET RELATIONSHIP



Lib Owned / Multi Inst = VPT Dependency

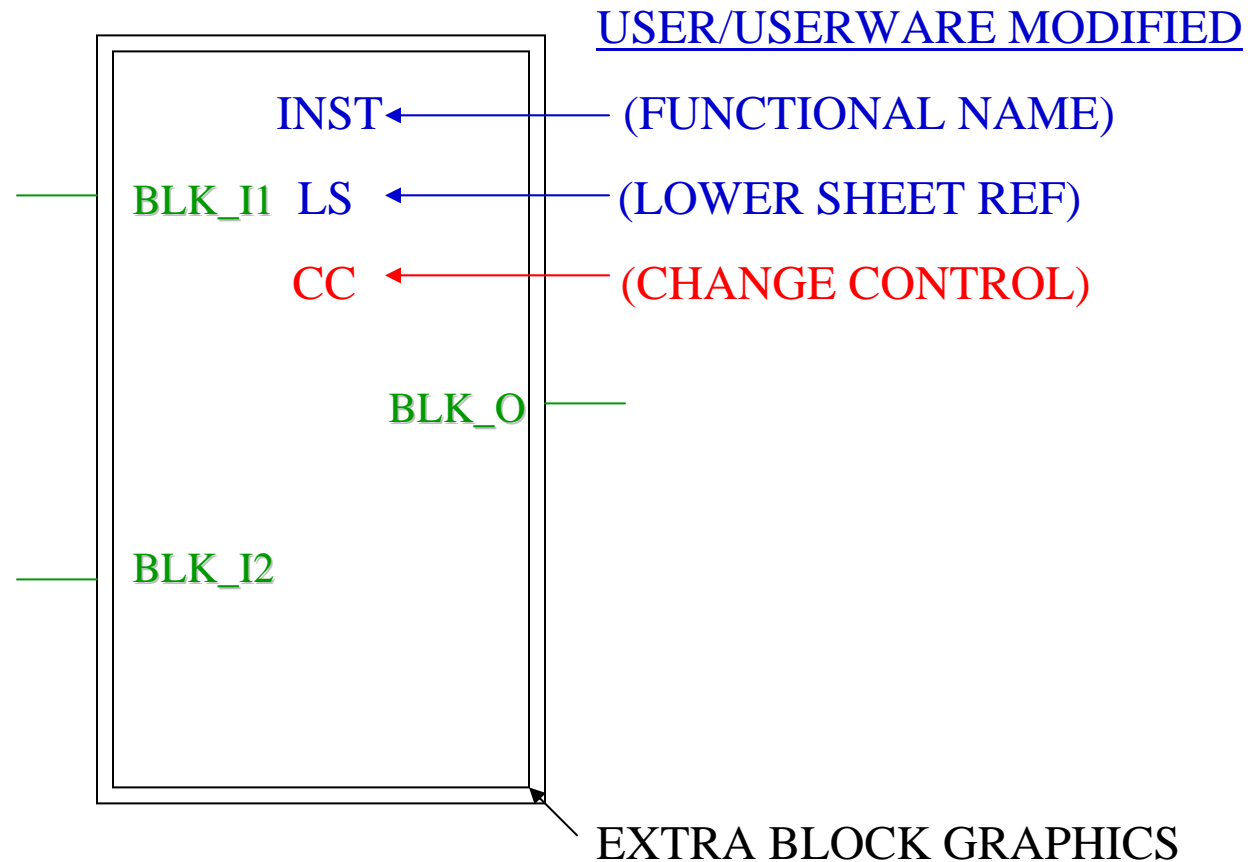
PRIMARY CONCEPT:
 THE VPT PROVIDES PROP
 MANAGEMENT, LAYERING
 OVERRIDE VALUES.
 REQUIRED FOR INSTANCE
 PROP VALUE UNIQUENESS



Block Creation Considerations

VISIBLE & VARIABLE BLOCK PROPS

VISIBLE & FIXED BLOCK PROPS



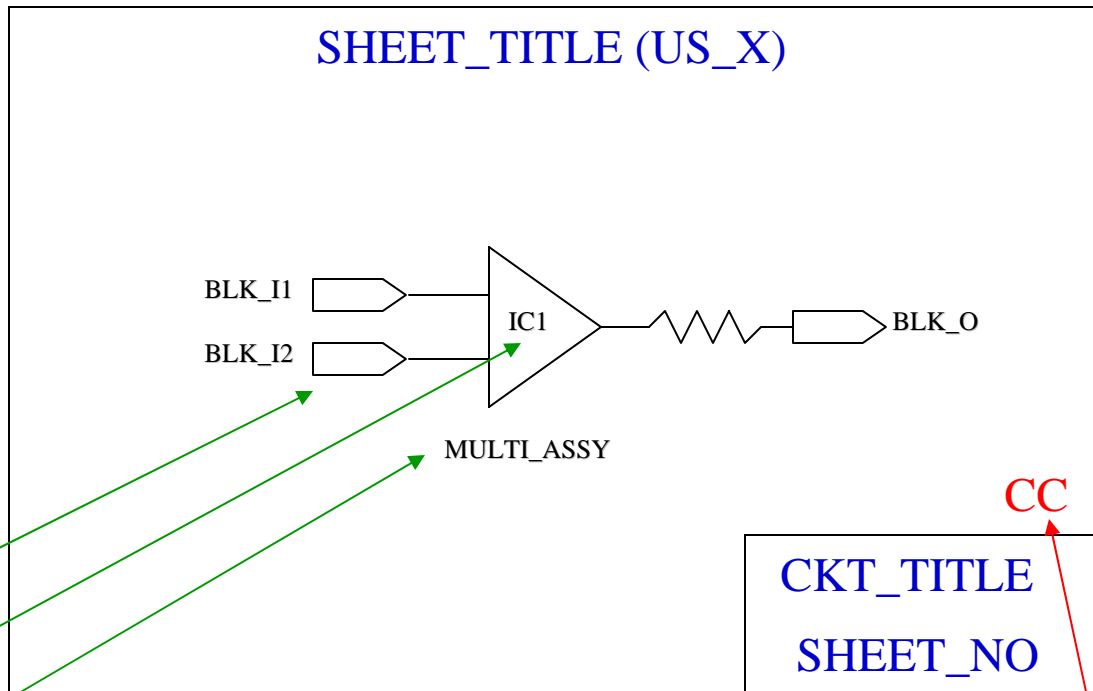
Underlying Sheet Creation Considerations

FIXED SHEET PROPS

VARIABLE SHEET PROPS
MUST ATTACH THESE
PROPS TO AN
INSTANCIATED SYMBOL
FOR FUTURE VPT EDITS.

ADD XREF SYMBOL?
PRESET REFDES?
SETUP VARIANTS TEXT?

US = UPPER SHEET REF



CHANGE CONTROL

Lib Block/Sheet Storage

- √ **LMS Based**
 - **Project Block Lib**
 - **Block Parts Menu**
 - **Distribution**
 - **Blocks Similar to Parts**
 - √ **Catalog Entries**
 - √ **Versioned Objects**
 - **Underlying Sheets Directly Linked**
 - √ **Changes Realized Immediately**

Lib Blocks on Design Sheets

- ✓ **Work Strictly in Design Context (VPT)**
- ✓ **Select / Add from Menu (Same as Parts)**
- ✓ **Customize Props (User or Userware)**
 - **Block (ie. Inst Prop)**
 - **Underlying Sheets (ie. Refs?, Doc – U/UW/BA)**
- ✓ **Same Block Maintenance**
 - **Blocks: Out_of_date Checking, LMS_update**
 - **Underlying Sheet: Automatic**
- ✓ **Changing Blocks**
 - **Results in Loss of All the Underlying Sheet Prop Overrides. Requires User/Userware Reset.**
- ✓ **Compounded ECOs – Design vs Blocks**

Limited Physical Reuse Experience

- ✓ **Implemented Later in the Project Life Cycle on 2 Blocks.**
 - **Difficult to Retrofit.**
- ✓ **Some Basics...**
 - **Create and Maintain Blocks PCB under LMS .**
 - **Maximize Outer Layer Routing for Application Considerations.**
 - **Board_Architect (BA) Required to Forward Place/Routing.**
 - **In Layout, Comp Group Entity. User Choice to Smash.**
- ✓ **Issues...**
 - **Blocks Did Not Update. Un-place and Re-place Work Around.**
 - **Awareness & Dependencies (ie. Vias/Tech_Rules)**
- ✓ **Given New Project Opportunity, Would Definitely Pursue.**
- ✓ **Mentor Appnote4623 – BA/BS Reuse Primer**
 - **<http://www.mentor.com/supportnet/member/appnotes/pdf/4623.pdf>**

Customization / Userware

- √ **Userware**
 - **Move / Enhance Functions for Design Context (VPT) Scope**
 - √ **Check Design (Sheet, Schematic, Doc, DVE)**
 - √ **Parts (Checks, BOM, Ref Files)**
 - √ **Printing**
 - √ **Misc (ie. Reports, Prop Management Functions)**
 - **For Source Scope, Disabled Output Functions Forcing Users to Generate in a Consistent VPT Mode.**
- √ **Hierarchical Flag Set in the Design Container.**
 - **Checkpoint for Various Custom Functions.**
 - √ **Merge Blocker**
 - √ **SRP Wrapper for Special Configs**

KEY TAKEAWAYS

- ✓ **Requires Considerable People, Planning and Process Efforts**
- ✓ **Highlights**
 - **Circuit Consistency**
 - **Positive Impact on Eng Circuit Inspection**
 - ✓ **Inspect and Certify Blocks Once.**
 - ✓ **Design Inspections Able to Ignore the Blocks.**
 - **Improved ECAD Design Efficiency**
 - ✓ **Initial Design Capture**
 - ✓ **Life Cycle Block ECOs**
 - **Systematic: Active Design & Deferred Designs**
 - **Positive Impact on Quality**
 - **No Additional Licenses / Costs.**
 - **Decreased Overall Schematic Interval and Cost by 20-30%.**

