

# Risk Mitigation in the Design of High Speed Digital – Analog Interfaces

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# Presentation is About:

- v **Informing the audience:**
  - **What major signal integrity tools are available**  
**From Mentor**
  - **Weaknesses and strengths of the various tools**
  - **Suggestions on where the applications of the tools**  
**are best suited**

# Presentation is About:

- ✓ **Suggesting a methodology to mitigate risk in high speed digital design and interfaces**
- ✓ **Presenting supporting material:**
  - **To compare simulated results with measured**
  - **To compare simulation results using IBIS models versus Spice models**
  - **Suggest when it would be good to use Spice models in addition to IBIS**
  - **Suggest a relatively simple process to obtain empirical results if it is deemed necessary**

# Presentation Outline

- ✓ *Overview of Signal Integrity Tools from MGC*
- ✓ **Basic Methodology**
  - **Tools to improve reliability of timing analysis**
- ✓ **Obtaining Empirical Data**
- ✓ **Application of Risk Mitigation procedures on actual programs**
- ✓ **Suggested Process Flow for Risk Mitigation**
- ✓ **Analysis for the Program Z**
- ✓ **Summary**
- ✓ **Questions/Comments**

# Overview of SI Tools

- ✓ **MGC has provided tools to analyze signal integrity. Major ones are:**
  - **Hyperlynx Software Suite**
    - ✓ **LineSim Options for pre-route analysis**
      - Crosstalk
      - Advanced Scope
      - Lossy Lines
      - Spice Output (NGC Beta-site tester)
    - ✓ **BoardSim Options for post-route analysis**
      - Crosstalk
      - Advanced Scope
      - Lossy Lines
      - Via Models
  - **ICX Software Suite**
    - ✓ **Offers both pre-route and post route analysis**

# Overview of SI Tools

- ✓ **Hyperlynx Tools covers ~95% + of signal integrity needs**
  - **Point-n-Click Interface is easy to use, making it far more likely that engineers will use**
- ✓ **ICX Tools**
  - **More powerful than Hyperlynx but more difficult to use and thus far fewer engineers have used this tool**
- ✓ **When to use ICX**
  - **Very critical designs, dense routing**
  - **When one must know how signals on different signal layers interact with each other**

# ICX

- ✓ **Powerful Batch Simulation Capabilities**
- ✓ **Design Capability**
  - **Component Placement**
  - **Automatic and Manual Routing**
  - **Real Time simulation updates during placement and routing**
  - **Changes go back to host CAD tool**

# ICX

- ✓ **Bi-Directional Link to timing analysis tools**
- ✓ **Spice (Eldo, Hspice), VHDL and IBIS modeling capability standard**
- ✓ **Scripting language for automation or adding user menus**
- ✓ **Corner Case**
- ✓ **Drag and Drop Waveform Analyzer**
- ✓ **Split Power Planes, Area Fills taken into account (V 3.4)**

# Overview of SI Tools

- ✓ **Results in this presentation from Hyperlynx**
  - **LineSim**
    - ✓ **Lossy Line**
    - ✓ **Advanced Scope**
    - ✓ **Spice Output**
  - **BoardSim**

# Presentation Outline

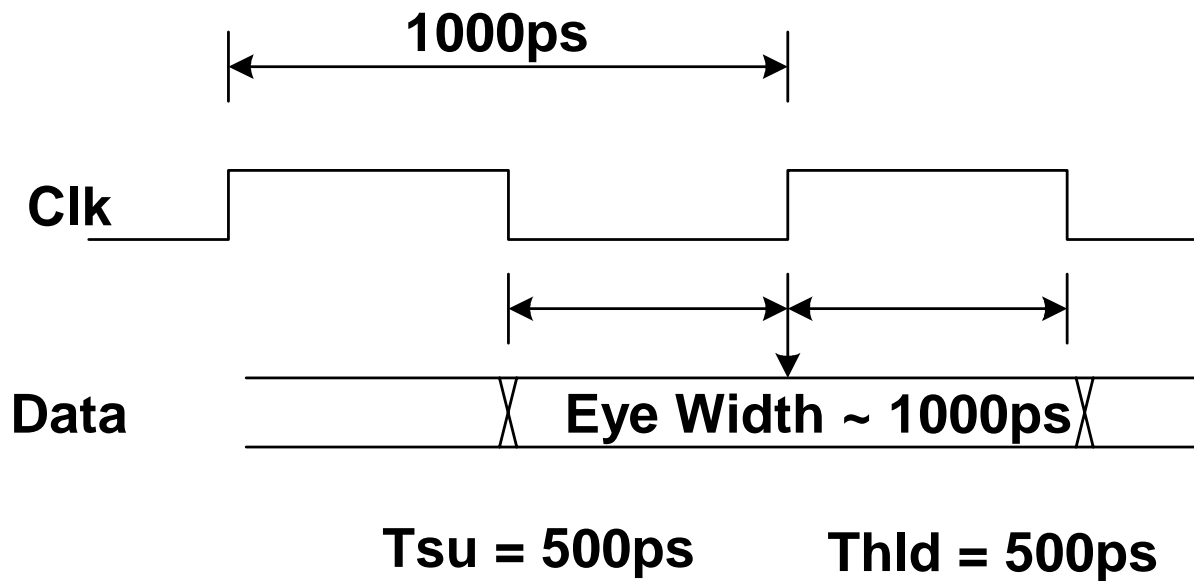
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# Basic Methodology

- ✓ **Paper Design**
  - **Timing analysis and budget**
- ✓ **Simulation**
  - **Pre-route**
  - **Post-route**
- ✓ **Obtain empirical data and compare with simulated results**
- ✓ **Iterate through the first three steps**

# Paper Design

- ✓ **Paper Design**
  - Begins with timing analysis
- ✓ **Basic Example**



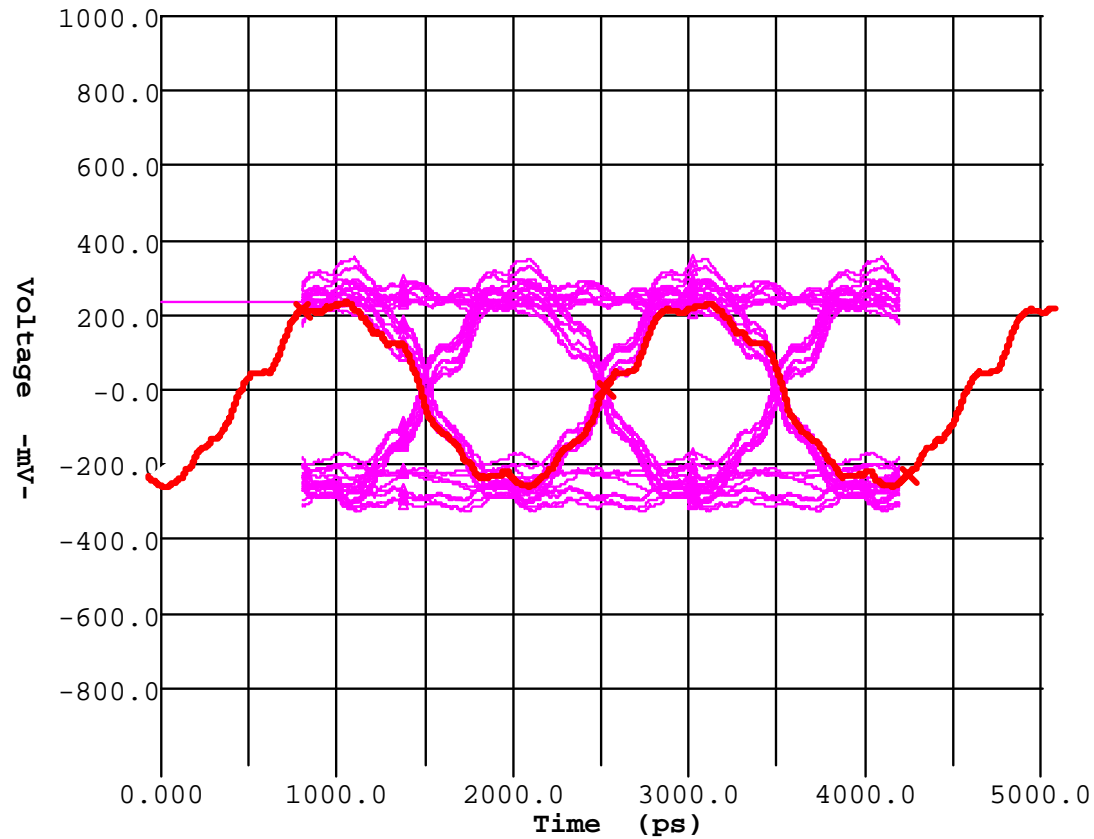
# Paper Design

- ✓ **Timing analysis, pitfalls:**
  - The anticipated “eye width” and signal amplitude is ideal
  - Thus the anticipated  $T_{su}$  and  $T_{hld}$  margins are ideal
  - In reality, the designer **MUST** know what the actual eye width is expected to be to obtain a useful timing budget
- ✓ **Signal integrity tools can help greatly**
- ✓ **In addition, rapid prototyping and empirical measurements allow for empirical verification**

# Advanced Scope Feature

- ✓ **Before Advanced Scope, Clock and Data signals simulation outputs treated the same**
- ✓ **Deceiving, because non-periodic wave forms behave differently from periodic**
- ✓ **Thus, the effect on eye width was not often accurate**

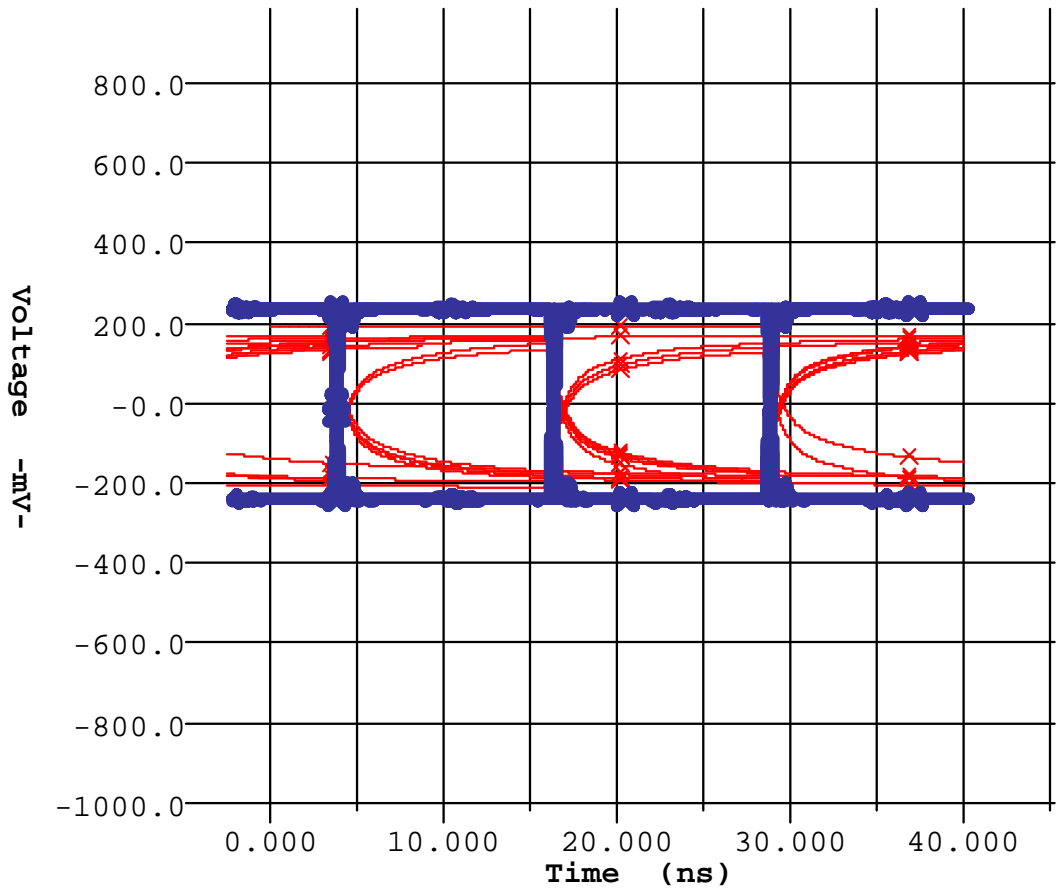
# Advanced Scope: Superimposed Waveforms



# Lossy Lines Feature

- ✓ **Before Lossy Lines, no difference in signal amplitude regardless of signal, or cable length**
- ✓ **Deceiving, because not only does the “eye width” become narrower, the signal amplitude may be too low for the receiver**

# Lossy Lines Feature



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# How can actual digital waveform measurements be made?

- v R/E Department has a *dedicated* test station made up of integrated digital, analog, and RF equipment to provide following capabilities:
  - Universal Analog to Digital conversion testing
  - Universal Digital to Analog conversion testing
  - High speed pattern generation/data acquisition for signal integrity testing, measurement and capture
  - 20GSPS Scope to capture high speed digital signals

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# Program X

- ✓ **Requirement:**

- **Is it possible to properly drive LVDS data at 80MBPS over 20' of ribbon cable?**

- **If not:**

- ✓ **This is program requirement. MUST verify that this can be accomplished!! Would mean interface redesign if not!!**

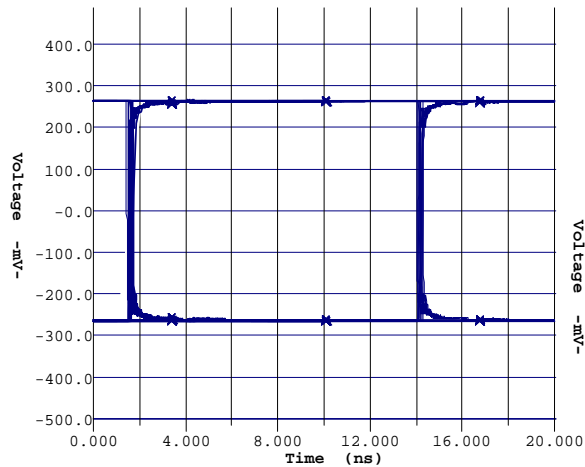
# Program X

## ✓ Procedure:

- Obtain IBIS models for driver, receiver, and cable
- To address concern about IBIS models for LVDS drivers (IBIS models are voltage driven, LVDS drivers are current devices):
  - ✓ Obtain SPICE Models for driver, receiver, and cable and run SPICE simulations
  - ✓ Verify if IBIS models for LVDS drivers are accurate
  - ✓ Set up experiment in lab using actual hardware and obtain empirical data

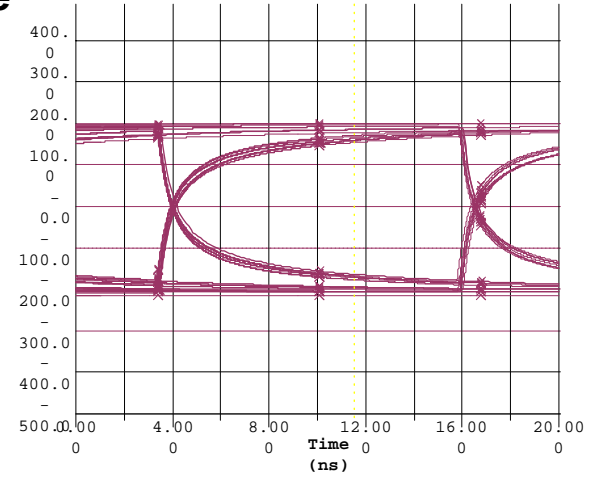


# Simulated Baseline: Spice

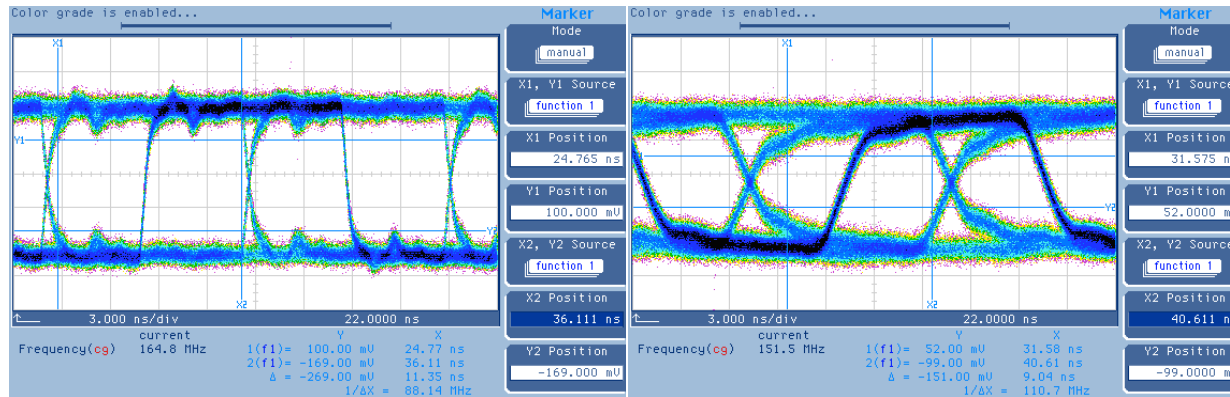


Baseline: 4" cable, no grounds between signal pairs

Spice

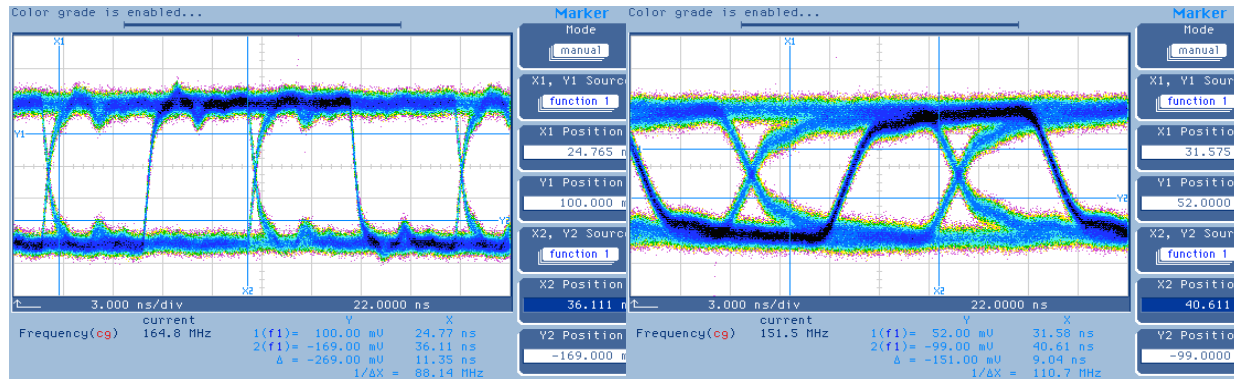
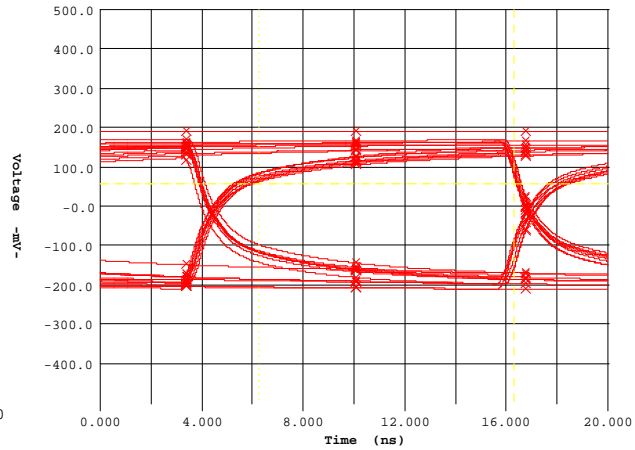
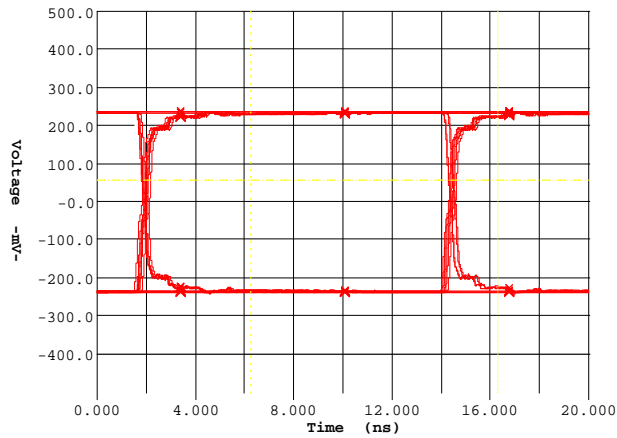


20' Cable: no grounds between signal pairs



Measured

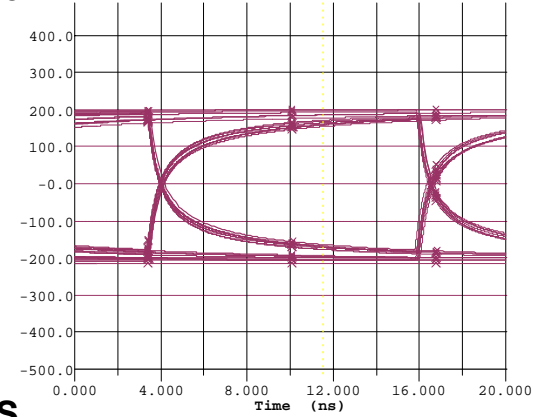
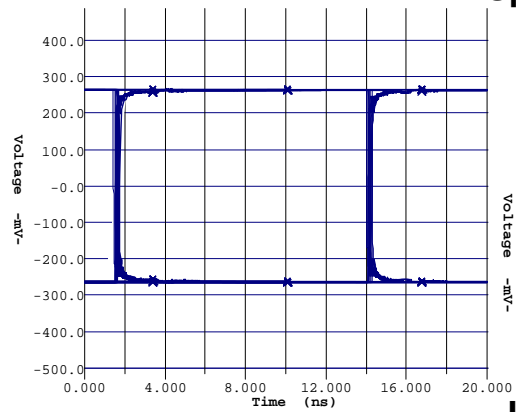
# Simulated Baseline: IBIS



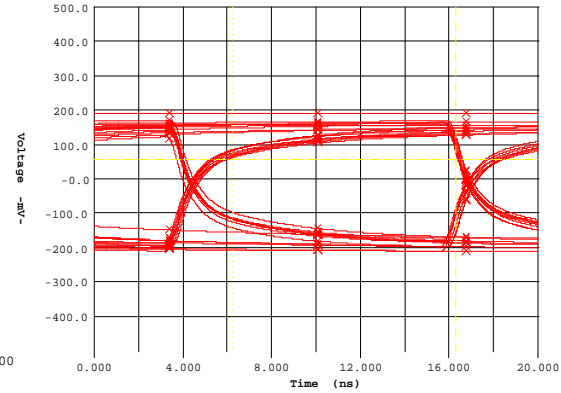
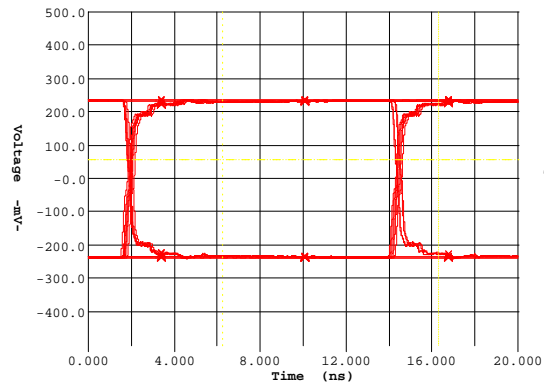
Measured

# Spice vs. IBIS

Spice



IBIS



# Program Y A/D

## v Problem

- Although A/D converter is spec'd at 1500MHz, the program requirement was for it to operate at 1800MHz

## v Issue

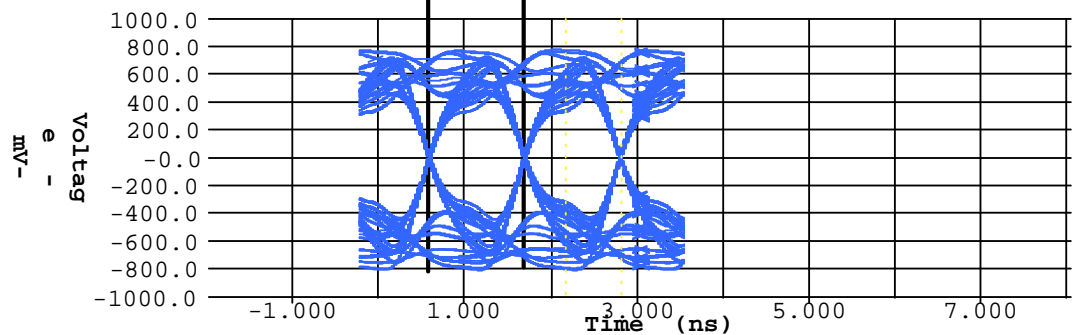
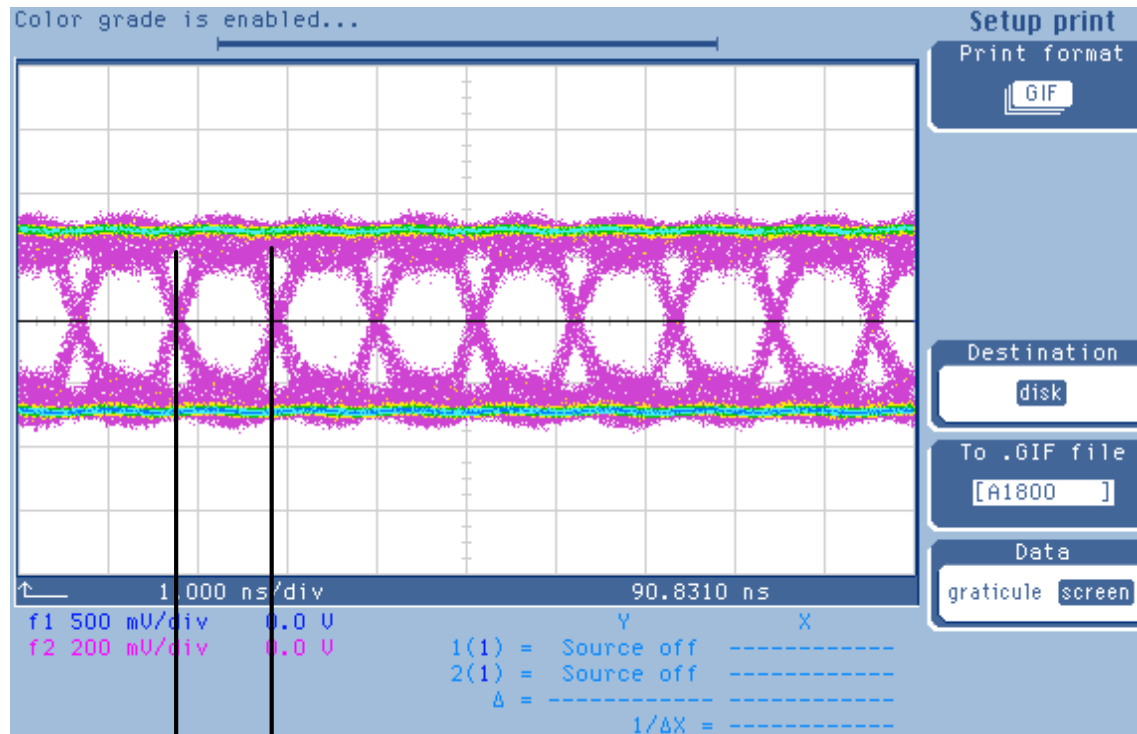
- Testing showed failures at 1800MHz, why?
  - v Is it the PCB construction?
  - v Is is the A/D?
  - v Finger Pointing!!!!

# Program Y A/D

- v **Procedure**
  - **Obtain IBIS models**
  - **Run simulations:**
    - v **Observe SI effects**
    - v **Observe “eye pattern”**
  - **Obtain measured data**
    - v **Compare results**
    - v **Decide next approach**

# 900MBPS Measured vs. Eye Builder

Actual Eye Pattern:  
900MBPS



Simulated Eye Pattern:  
900MBPS

# Program Y A/D

## ✓ Resolution

- Because simulation results were so close to measured

- ✓ Confidence in additional simulations

- ✓ Indicated that the culprit was more likely the A/D converter

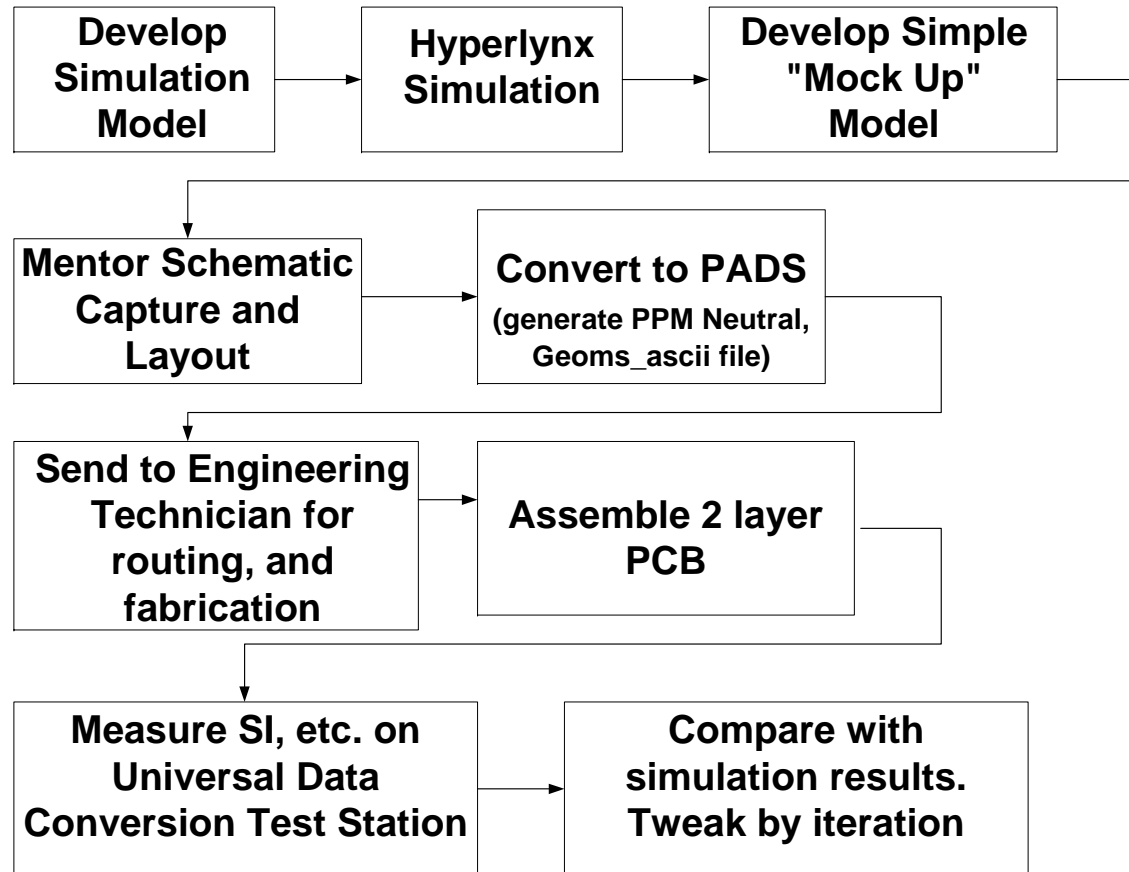
- SI looked good

- Eye pattern indicated that timing and voltage swing were adequate

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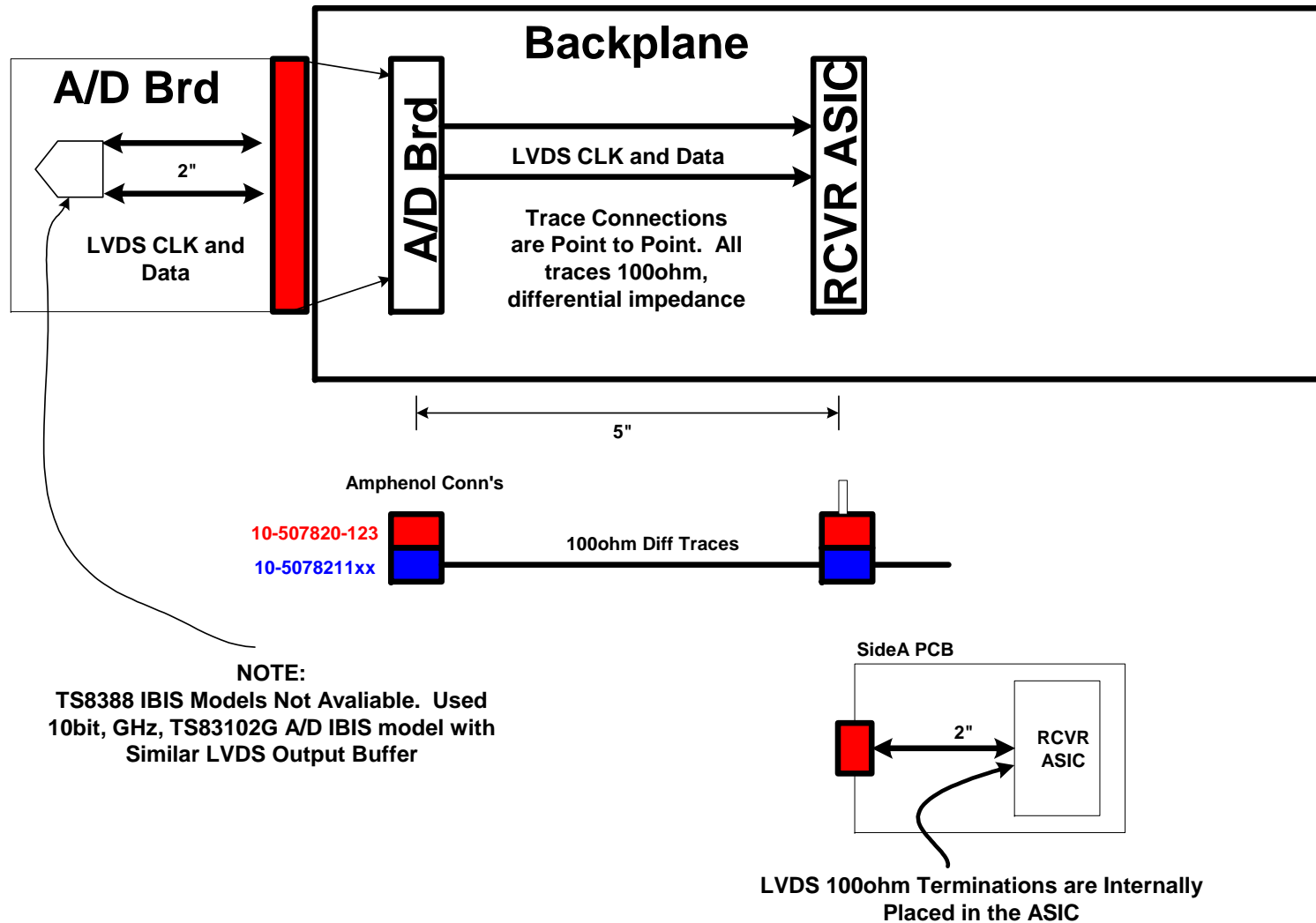
# Suggested Process Flow for Risk Mitigation



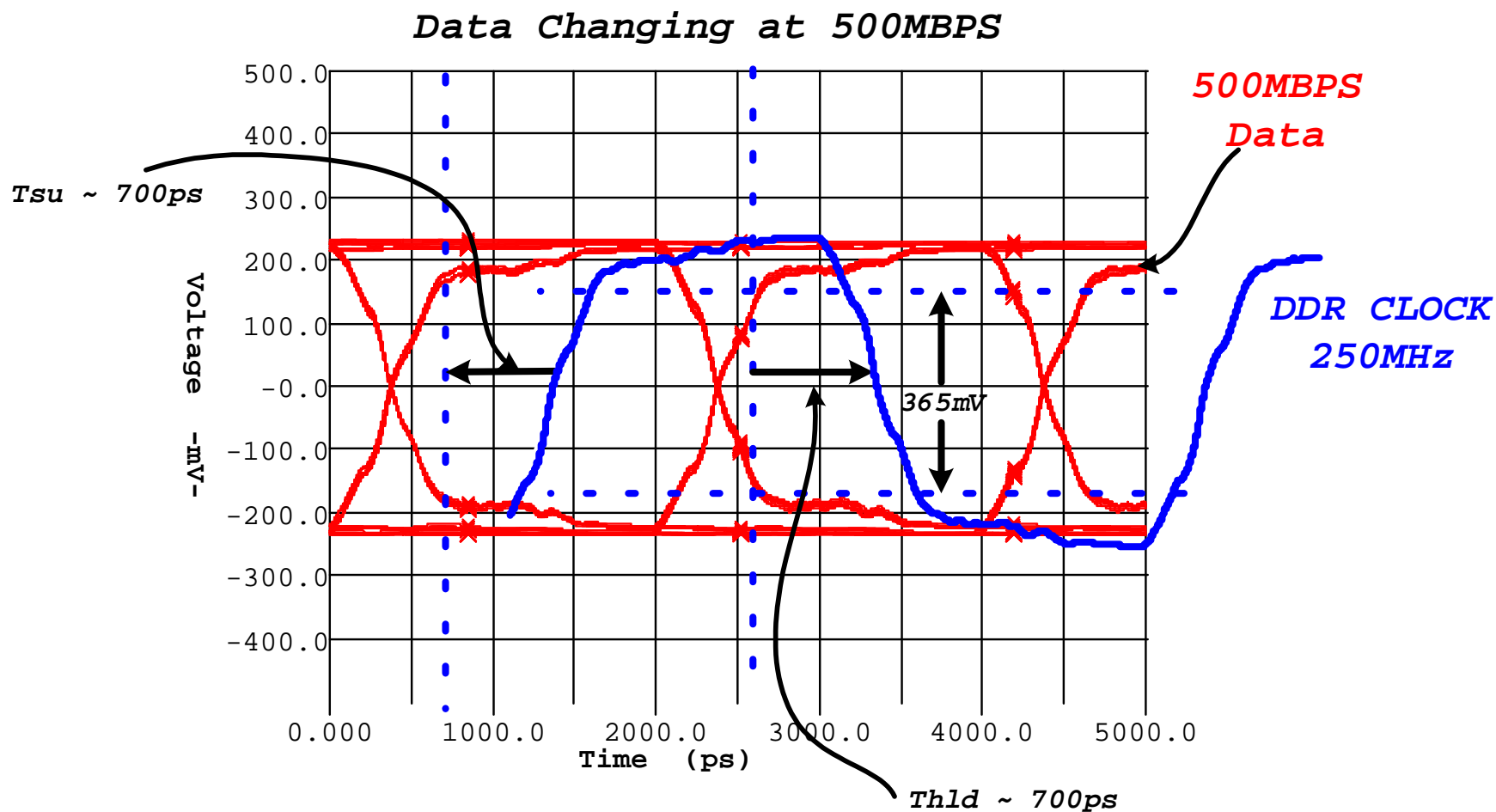
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# Model of A/D Interface



# Simulation Results: Superimposed DDR CLK and Data Outputs



# Recommended Routing Rules: A/D ASIC Interface

- v **Assuming:**
  - **Tsu & Thld of the receiving ASIC is +/- 100ps:**
  - **Dielectric constant = 4.3, and thus Tprop ~175ps/in nominal**
  - **A/D Output clock center samples data output**
- v **Referenced to the A/D output clock (DR, DRB)**
  - **Data paths should be routed +/- 1.0 inches MAX; i.e. no data path should be longer than or shorter than 1” from the clock path**
    - v **This means the entire path, from the A/D output right up to the ASIC input**
    - v **This is your timing budget**

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# Summary

- ✓ **Simulation in Hyperlynx with IBIS models using the “Lossy Line” and “Advanced Scope” features in Hyperlynx closely matched both**
  - **SPICE simulation results**
  - **Measured Data**
- ✓ **Usage of SPICE models in Hyperlynx,**
  - **SPICE models are more accurate than IBIS but close**
  - **Spice simulations in Hyperlynx take much longer**
  - **Better to use SPICE models to verify IBIS models**
  - **Once verified, use IBIS models**

# Summary

- ✓ **After identifying critical signals, and/or interfaces**
  - **If you are concerned with**
    - ✓ **Signal integrity issues**
    - ✓ **Accurate timing margins**
    - ✓ **Developing realistic design constraints**
  - **You do not have to**
    - ✓ **Guess**
    - ✓ **Rely on “rules of thumb”**
    - ✓ **Fall back on, “well that’s the way someone else did it before”**
    - ✓ **Force the PCB designer to cover for you because you did not take the time and effort to develop realistic design constraints based on good simulation results and/or empirical data**

# Summary

- ✓ **After identifying critical signals, and/or interfaces**
  - **You can:**
    - ✓ **Develop a model of your system that includes all the discontinuities you can identify**
    - ✓ **Obtain IBIS and if necessary SPICE models**
    - ✓ **Use the Lossy Line and Advanced Scope features, accurately predict timing margins to develop realistic timing design constraints**
    - ✓ **For especially critical interfaces, design simple hardware prototypes that can be quickly fabricated, and then tested using high bandwidth scopes to confirm simulation results**

# Questions/Comments