

Using Innovative Tool Capabilities in ICX

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MARLUG - Mid-Atlantic Region Local Users Group
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Agenda

- v **Understanding ICX simulations**
- v **SDF and BDF for timing constraints**
- v **Understanding Allocation**
- v **Debugging simulation issues**
- v **Debugging IBIS Models**
- v **Differences between Simulators**

Simulation Steps

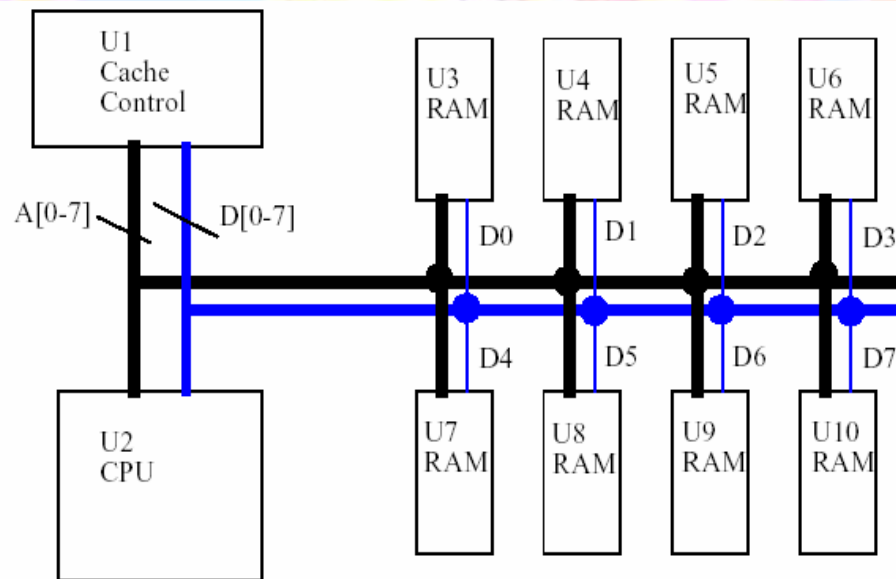
- ✓ **Component Modeling**
- ✓ **Trace Modeling**
- ✓ **Field Solver**
- ✓ **Reporting Results**

Component Modeling

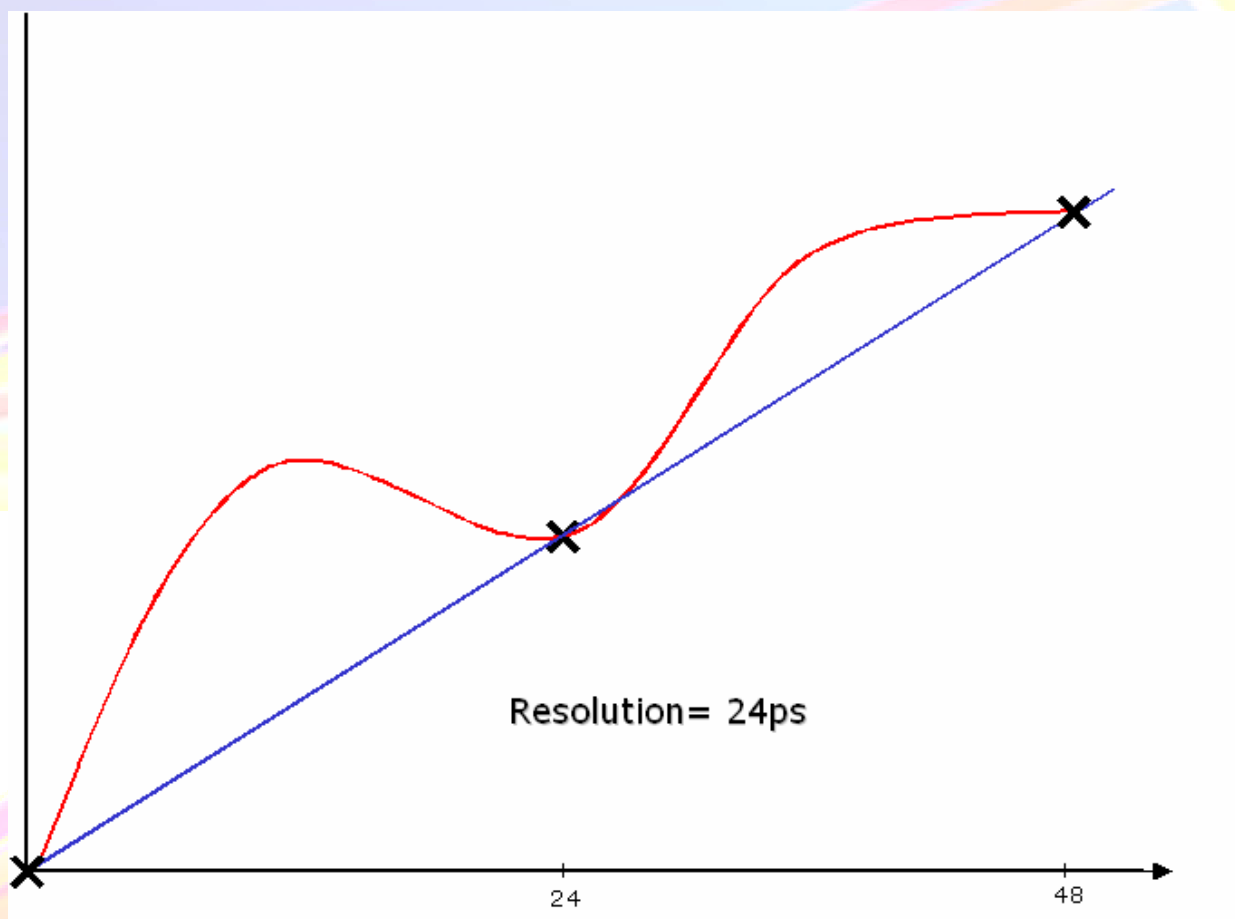
- ✓ **Overall Accuracy**
 - **Garbage In = Garbage Out**
- ✓ **Incorrect data can “confuse” the simulator**
 - **Nonmonotonic behavior (Rising or Falling)**
- ✓ **Anomalies can result in singularity Errors**
- ✓ **Models on Coupled Nets**
- ✓ **Models affect Performance (# of points)**
- ✓ **Long initial delay in VT curves (more later)**

Getting The Model Type Correct

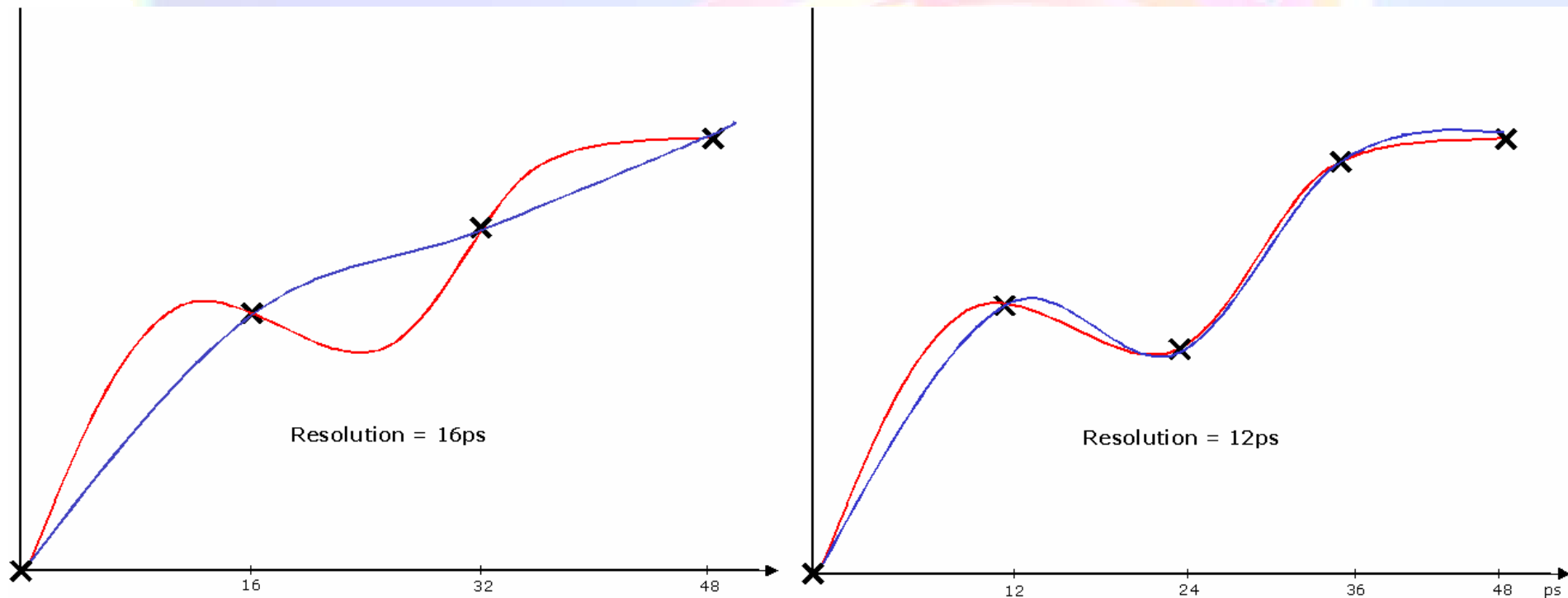
- ✓ Is the pin really bi-directional
- ✓ Unnecessary simulations
 - Number of driver combinations for Delay and Crosstalk.
- ✓ More complex DC solutions
- ✓ More complex coupling



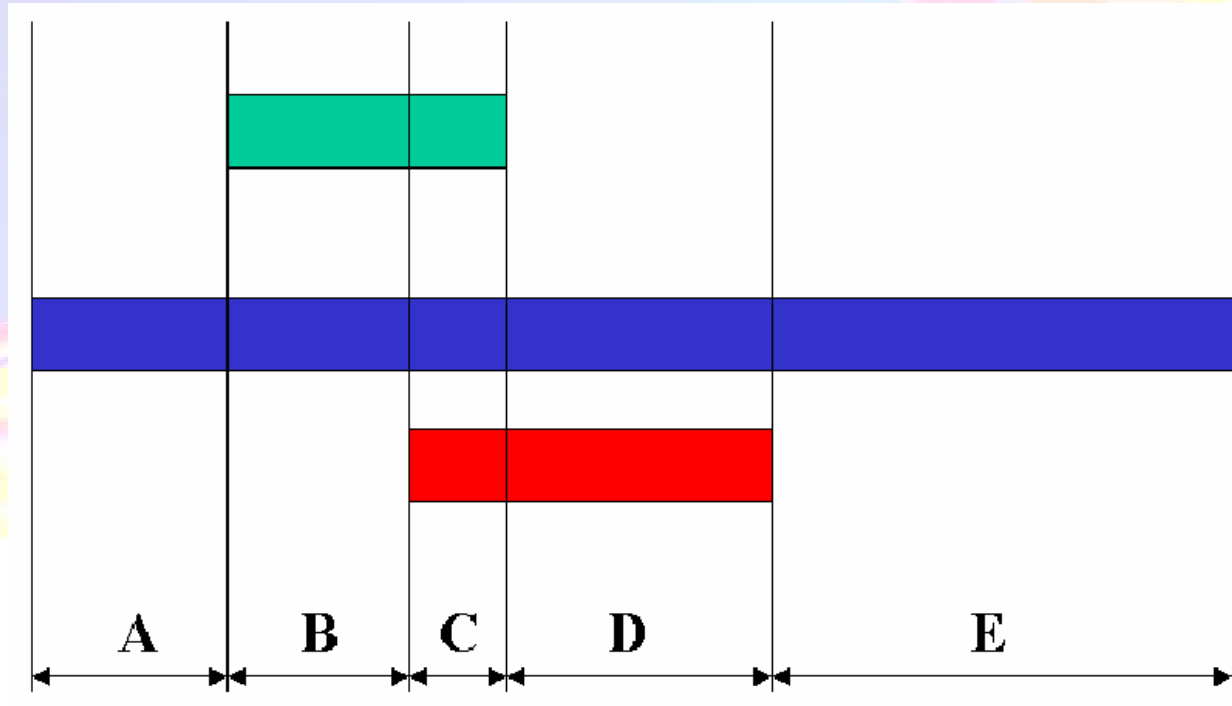
Impact of Time Resolution



Impact of Time Resolution



Initial Trace Extraction

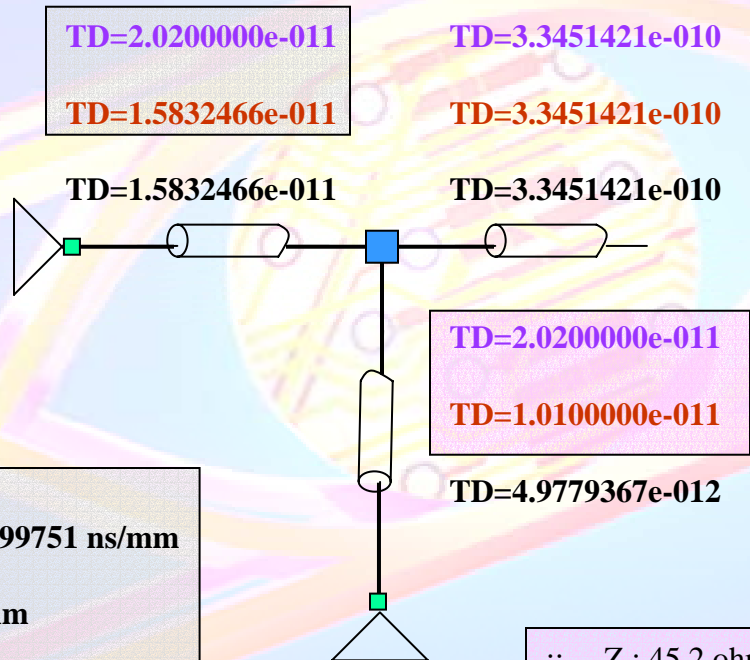


- ✓ Searches for traces within the Horizontal Coupling Distance
- ✓ Must fit within Horizontal & Vertical Neighbor Limits.
- ✓ Broken into unique cross sections.
 - ❖ $\geq 50\%$ of Time Resolution expanded to 101%
 - ❖ $< 50\%$ of Time Resolution removed

Simulatable Trace Model

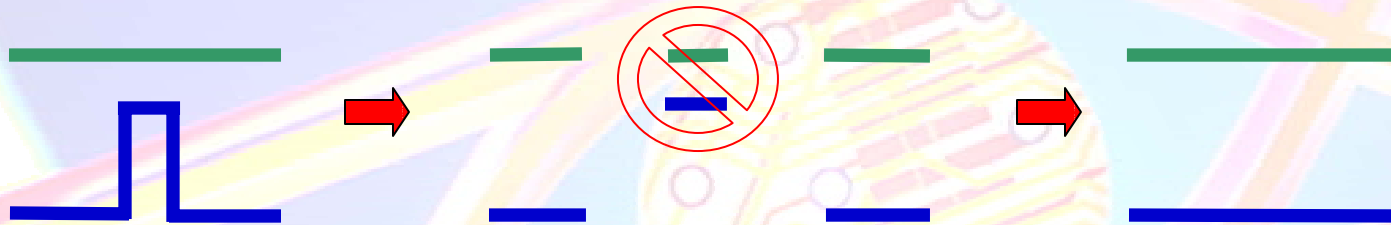
Resolution

20ps
10ps
1ps



Simulator Internal Adjustments

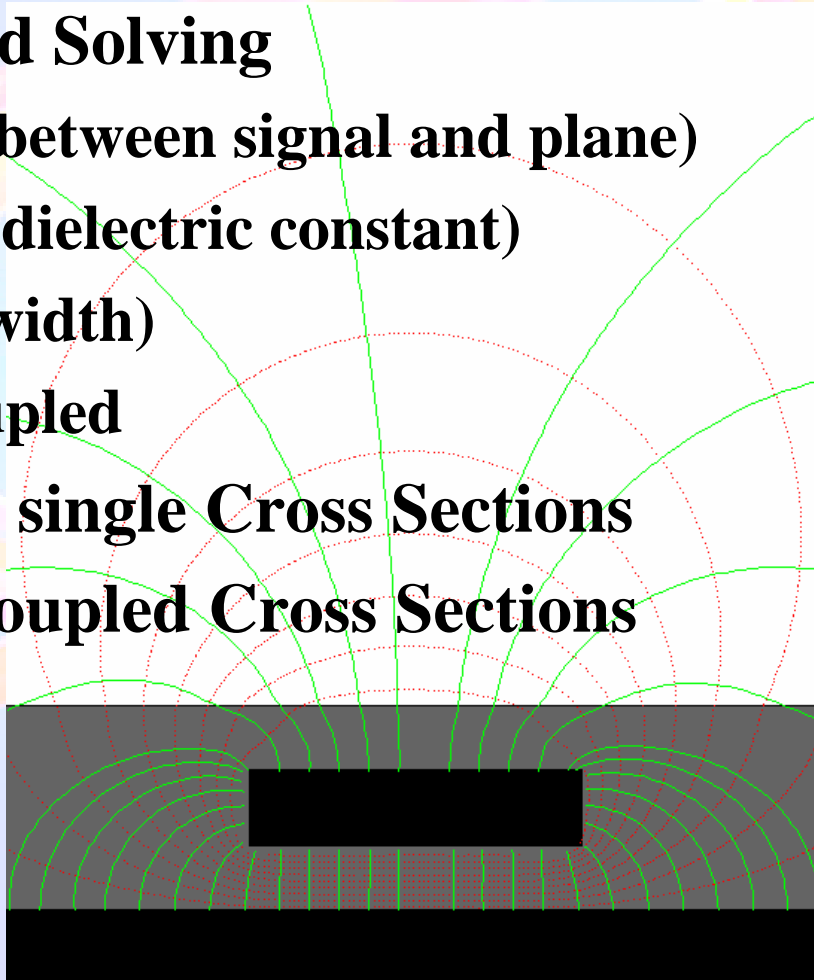
- Adjacent “Like” cross sections are merged.



- The final cross section must be a multiple of the resolution.
- Lengths which were stretched to 101% are then brought back to 100%

Field Solving

- ✓ **Setup Affecting Field Solving**
 - Stackup (distance between signal and plane)
 - Material (loss and dielectric constant)
 - Trace Geometry (width)
 - Coupled vs. Uncoupled
- ✓ **Pure Impedance for single Cross Sections**
- ✓ **Matrix values for Coupled Cross Sections**



Reporting the Results

- ✓ **Reported results are +/-50% of resolution**
 - **Delay reported to 1ps**
 - **SI reported to 0.01mV**
- ✓ **Checking uses resolution for tolerance.**
 - **For example**
 - ✓ **Min Delay Constraint = 1.0ns**
 - ✓ **Time Res = 50ps**
 - ✓ **Reported Delay = 0.976 (no error)**
 - ✓ **$0.976\text{ns} + 50\text{ps}/2 = 1.01\text{ns}$**

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Pin To Pin Timing Constraints

- ✓ **Devices**

- 4 SDRAMs
- 2 DSPs
- 1 Xilinx FPGA

- ✓ **Example Bus**

- Address (0-13)

- ✓ **Total number of user entered and maintained constraints**

- 168

BDF/SDF Timing Constraints

- v **Same Example**
 - 3 BUSPORTDEFS
 - 7 BUSPORTS
 - 12 Timing constraints
- v **Benefits**
 - Easier to maintain
 - Faster to load
 - Better reuse possibilities
- v **SDF from Tau or external sources**
 - Tau is MGC's Symbolic timing analyzer

Example Files

```
BUSPORTDEFS
FORMAT "PIN"
("U34000" "U34001" "U34002" "U34003")
"SDRAM_ADDR" "23" "24" "25" "26" "29" "30" "31" "32" "33"
"34" "22" "35" "20" "21";

("U33000" "U36000")
"DSP_ADDR" "M24" "M23" "N26" "N24" "N23" "P26" "P24"
"P23" "R24" "R23" "T26" "T25" "U26" "U25";

("U48000")
"FPGA_ADDR" "AL11" "AK11" "AL12" "AK12" "AJ13" "AK13"
"AL13" "AK14" "AK15" "AK26" "AK10" "AK27" "AK9" "AL10";

BUSPORTS
"U34000"
"SDRAM_ADDR" "ADDR[0:13]" "23" 0:13:1
;
```

```
(DELAYFILE
(DESIGN " DESIGNNAME")
( DATE "" )
(VENDOR "Mentor Graphics Corporation")
(PROGRAM "tau")
(VERSION " n.n")
(DIVIDER /)
(VOLTAGE 4.5:5.0:5.5)
(PROCESS "worst")
(TEMPERATURE 55:85:125)
(TIMESCALE 1ns)

(CELL
(CELLTYPE "system")
(INSTANCE design)
(TIMINGCHECK
(PATHCONSTRAINT
(INSTANCE U33000) ADDR\[0\:13\]
(INSTANCE U34000) ADDR\[0\:13\]
(-0.5::2.000)
)
)
```

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Absolute Rules

Edit>RulesEditor>Electrical>Timing

constrainable item	min actual	min rule	min alloc	max actual	max rule	max alloc	visibility
net1	1	1	1				
net2	2	2	2				
net3	1.6	3	3				

constrainable item	min actual	min rule	min alloc	max actual	max rule	max alloc	visibility
net1	1				1	1	
net2	2				2	2	
net3	1.6				3	3	

- ✓ **Allocation when absolute min rule is set is the same as min rule**
- ✓ **Allocation when absolute max rule is set is the same as max rule**

Single Ended Relative Rules

Edit>RulesEditor>Electrical>Timing

constrainable item	min actual	min rule	min alloc	max actual	max rule	max alloc	visibility
net1	1	a	2				
net2	2	a	2				
net3	1.6	a	2				

constrainable item	min actual	min rule	min alloc	max actual	max rule	max alloc	visibility
net1	1		2.2	2	a	3.2	
net2	2		2.2	3	a	3.2	
net3	1.6		1.6	3.2	a	3.2	

- ✓ **Relative min rule with no max rule means match to delay tolerance (time resolution)**
- ✓ **Relative max rule with no min rule means match to delay tolerance (time resolution)**
 - **Min allocation is Max Alloc – delta(Max Actual,Min Actual)**

Relative Max Rule & Associated Min Rule

Edit>RulesEditor>Electrical>Timing

constrainable item	min actual	min rule	min alloc	max actual	max rule	max alloc	visibility
net1	1	a	2.2	2	a+1	3.2	
net2	2	a	2.2	3	a+2	4.2	
net3	1.6	a	2.2	3.2	a+1	3.2	

constrainable item	min actual	min rule	min alloc	max actual	max rule	max alloc	visibility
net1	1	a	2.2	2	a+1	3.2	
net2	2	a+1	3.2	3	a+2	4.2	
net3	1.6	a	2.2	3.2	a+1	3.2	

- v **Max rule is the maximum of the maximum delays**
- v **Min delay is extracted from the rule**
 - **If rule is tighter than ramp time of receiver – allocation error**

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Expectations

- ✓ **Accuracy expectations**
 - “Expected” results do not always match reality
 - Reducing coupling can increase crosstalk
 - Increasing coupling can reduce delays
- ✓ **Performance expectations**
 - Perceived performance
 - Actual performance
 - Know when to carry out what type of simulations
- ✓ **Reducing the uncertainty in results**

Using The Best Timing Resolution

- ✓ **The component model**
 - Target 20 points within 20% - 80% rise time
- ✓ **The traces themselves**
 - Termination placement
 - Propagation delay
 - Manufacturing rules for routing
 - ✓ Minimum segment lengths

If Some IS Good – Is More Better ?

- v **Coupling**
 - **Sensible limits, rather than exhaustive**
 - **Area Fill detection is not affected by**
 - v **Horizontal Neighbor Limit**
 - v **Vertical Layer Limit**
- v **Impacts of loss**
 - **Frequency**
 - **Optimistic or pessimistic views of the world**
- v **Not every corner is needed for full verification**
- v **ADMS is faster than SPICE, but not IBIS**

Narrowing the Issue

- ✓ **Limitations of the model we are using**
 - DC losses, via modeling and very fine resolution
- ✓ **Modeling chain**
 - Component
 - Trace
 - Field Solver
- ✓ **Reporting Anomalies**

Modeling Chain

- ✓ **Component**
 - IBIS Editor
 - Exported model vs. imported model
 - NC model some of the parts of the system
 - Can we reproduce it in simple EE design
 - Can we reproduce with a known good model
- ✓ **Trace**
 - What does the simulation look like uncoupled
 - What does the simulation look like unrouted
 - SPICE netlist
- ✓ **Field Solver**
 - Are we at the edges
 - ✓ Materials, thicknesses

Reporting Anomalies

- ✓ **Look at the waveform**
 - Use toolkit if “Worst Case Crosstalk” needed
 - Monotonicity can cause unexpected results
 - Over-clocking issues
- ✓ **Checking waveforms**
- ✓ **“Actuals” log**

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Debugging IBIS Models

- ✓ **Parser catches syntax errors**
 - **Not always the whole picture**
- ✓ **Model checker provides Warnings**
 - **Non-Monotonic**
 - ✓ **Could be omitted unit designation**
 - ✓ **Can cause extra delay**
 - **DC Endpoints Mismatch**
 - ✓ **Extrapolation**
 - ✓ **Initial Delay**

Debugging IBIS Models

- ✓ **Initial delay in VT curves**
 - Most frequent issue
 - Algorithm to remove delay is based on first waveform
 - Handled differently among simulators
- ✓ **Editing issues**
 - Can safely remove a few points
 - Whole scale edit not a good idea if not model author
 - Cannot paste curves from one model to another

Advanced Modeling

Using the Advanced simulation capabilities

✓ ADMS

— What models are simulated with this simulator?

- ✓ VHDL-AMS, Eldo SPICE, Encrypted Eldo and HSPICE

— How do I know ADMS is being used?

- ✓ Waiting for the WDB server to start message

✓ HSPICE

— This simulator is required for Encrypted HSPICE models

— How do I prepare my environment?

- ✓ HSPICE must be installed
- ✓ `installdir` environment variable must be set
- ✓ HSPICE license must be available.

ICX_TOOLKIT

- ✓ **%MGC_HOME%\pkgs\icx\userware\ICX_TOOLKIT**
 - **IS_MultiBoard - Verify->X-Synchronize System**
 - ✓ **Querys the selected design for simulation parameters and then set these same parameters in all the other designs in the system.**
 - **File->Export->X-Generate RC Models**
 - ✓ **Creates IBIS model files for all the parts with reference designators, C* and R* that have one of the value properties, VALUE, INSTPAR, or SPICEPAR.**
 - **Options->X-Pulse Trains**
 - ✓ **Java utility to easily define long pulse trains by user defined bit patterns, random bits, automatic PRBS generator, or clocks.**
 - **And much more.....**

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Differences Between Simulators

✓ **Mentor Simulators**

- **ICX, HyperLynx, XTK and still some VBSA**

- ✓ **Different support of IBIS Constructs**

- **Model selector, diff pin**

- ✓ **Handling of Non-Monotonic points**

- **Remove, warn**

- ✓ **Remove initial delay**

- **Different algorithms = Different simulation results**

- ✓ **Timestep Calculation**

- **Auto vs user**

- ✓ **Handling of 0 length segments**

Help Available

- ✓ **Extensive Knowledge Base available**
 - Supportnet - <http://www.mentor.com/supportnet/>
 - Over 2500 technotes available for High Speed products
 - Animated Demos available – step by step
- ✓ **Talented Customer Support Team**
 - East and West time zone coverage
 - Over 20 years experience
 - Several folks with SI design experience
 - ✓ Not just tool jocks!

The image features the Mentor Graphics logo in a bold, white, sans-serif font. The logo is centered and set against a vibrant blue background. The background is filled with intricate, glowing white and light blue patterns that resemble circuit board traces, data lines, and geometric shapes. The overall aesthetic is high-tech and digital. The word "Mentor" is positioned above "Graphics", and a registered trademark symbol (®) is located to the right of the word "Graphics".

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