

Microprocessor Data Bus Signal Integrity Problem

Bell Labs

Innovations for Lucent Technologies

Jeffrey Cohen

Member of Technical Staff

Phone 973 386 6370

Fax 973 386 6503

Bell Laboratories
67 Whippany Road
Room 4C-334
Whippany, NJ 07981-0903 USA

jcohen1@lucent.com

Lucent Technologies



MARLUG - Mid-Atlantic Region Local Users Group
ANNUAL CONFERENCE - OCTOBER 5, 2004
Johns Hopkins University Applied Physics Lab – Laurel, MD

Outline

- ✓ **Signal integrity problems of microprocessor data bus.**
- ✓ **Example of a microprocessor data bus.**
- ✓ **Demonstration of ICX capabilities.**
- ✓ **Evaluation of the ICX output.**
- ✓ **Presentation of the implemented solution.**
- ✓ **Summary and conclusions.**

Microprocessor Data Busses

- v **Microprocessor data buses pose a signal integrity challenge.**
 - **System configurations have non-homogenous devices manufactured on different processes all connected to the same bus.**
 - **Because of slew rate and packaging differences similar devices, even from the same manufacturer may have significant differences in input and output characteristics.**

Signal Integrity Problem

- ✓ **Transmission line analysis and the termination synthesis feature of ICX can be used to solve this type of a problem.**
 - **There are tradeoffs between performance and the following;**
 - ✓ **Increased rise time.**
 - ✓ **Lower noise immunity.**
 - ✓ **Increased power consumption.**

Transmission Lines

- v **Transmission line: definition.**
 - **A circuit element that effects the signal transmission from node to node.**
 - **If the line length (in inches) is greater than the signal rise time (in nanoseconds) the line is considered a transmission line.**
 - **Line delay $>$ 20% of rise/fall time.**
 - **Output driver is at a steady state value, and the signal has not yet arrived at the destination:**

Transmission Line Reflection Coefficient

- v Transmission lines have a characteristic impedance.
 - If R_0 is the transmission line's characteristic impedance and R is the impedance at a node connected to the transmission line then the reflection coefficient ρ is the following.

$$\rho = \frac{\frac{R}{R_0} - 1}{\frac{R}{R_0} + 1}$$

Device Input Impedance

- ✓ **The assumption:**
 - All CMOS devices have high impedance inputs: $\rho = 1$ at the receiver.
- ✓ **The received waveform for an un-terminated transmission line.**
 - The initial received waveform will equal incident waveform plus the reflected waveform.
 - About two times the incident waveform.

What Is Rise Time?

- ✓ **Rate of change in output voltage vs. Time at a specified load, over the 10-90% marks of the transition region.**
- ✓ **Can be inferred from the device ibis model.**
- ✓ **PCI-2.2 has specified 1-4 v/ns.**
- ✓ **JEDEC JESD8-9B (DDR-II) : 1v/ns minimum.**

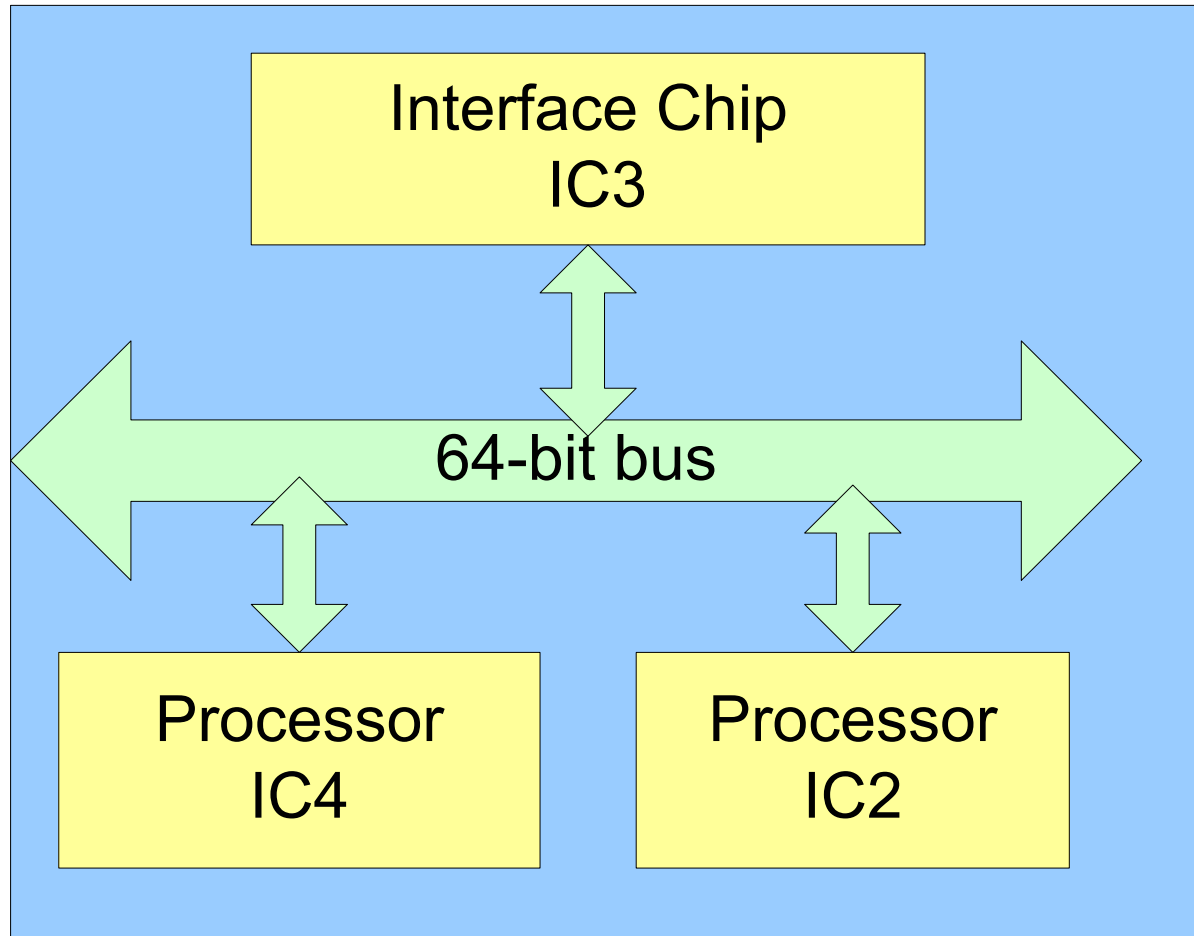
Launched Waveform

- ✓ **The waveform launched by the signal source is a function of the source current capacity and source impedance.**
- ✓ **The source impedance effects rise time.**
- ✓ **CMOS devices have a range of five to twenty ohms for source impedance.**

Rise Time and Reflections

- v **Rise time is related to launched waveform amplitude.**
 - **If $\rho = 1$ at the receiver, then two times the launched amplitude will be seen at the receiver.**
 - **Fortunately, the greater the initial launched amplitude, the lower the output impedance is, the larger the value of ρ will be at the source. This will reduce the ringing.**

Microprocessor Circuit Example



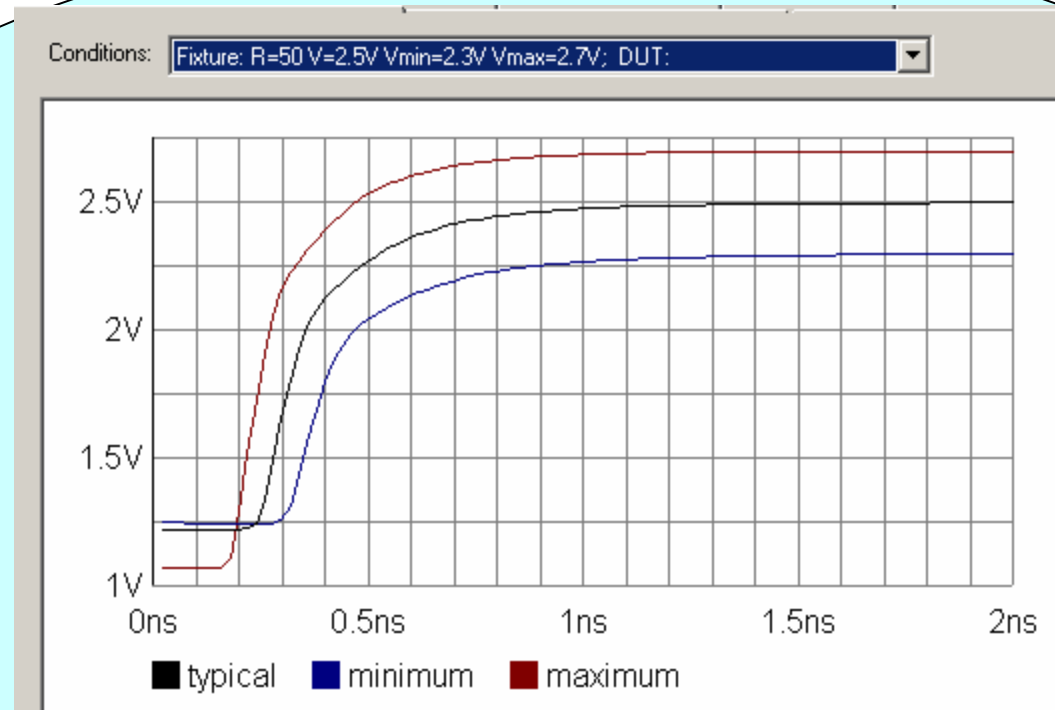
Microprocessor Circuit Example (Contd.)

- v **Bus speed 133 MHz.**
 - Transmission line length is 0.75 inch.
 - All traces have a characteristic impedance of 50Ω .
 - Parasitic differences in table below.

Parasitic	Processor	Interface Chip
Resistance	1.165 Ω	0.232 Ω
Capacitance	3.79pF	4.222pF
Inductance	6.118nH	4.222nH

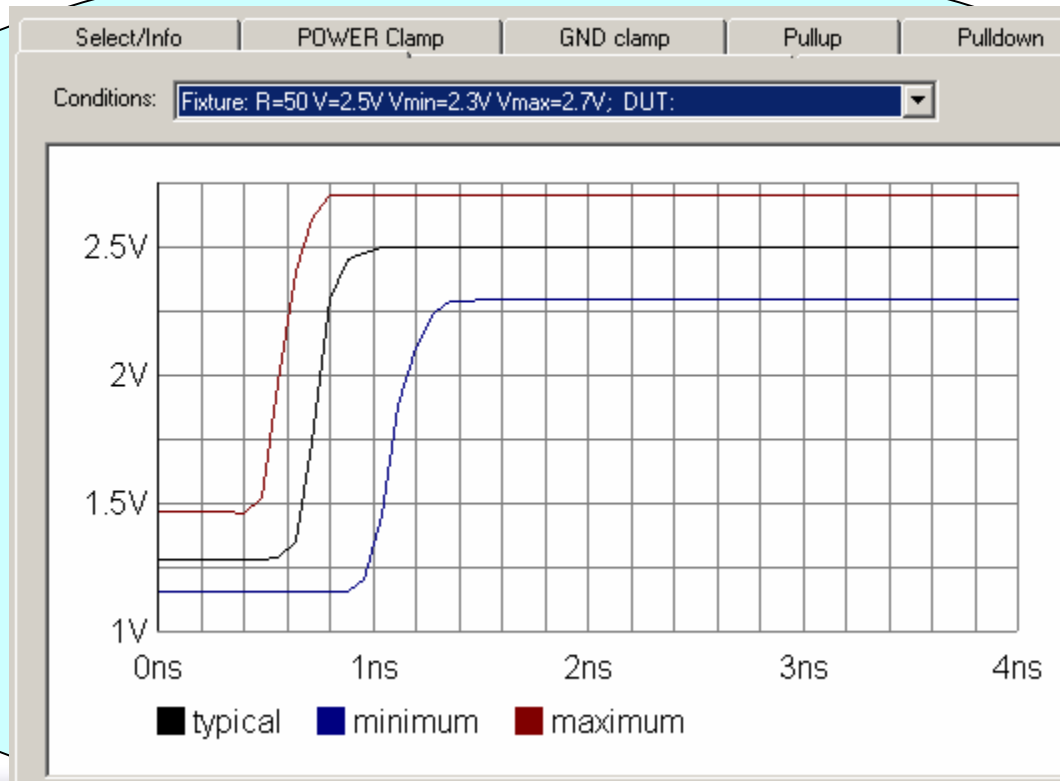
Slew Rates

- Processor: range 4-10 v/nS.

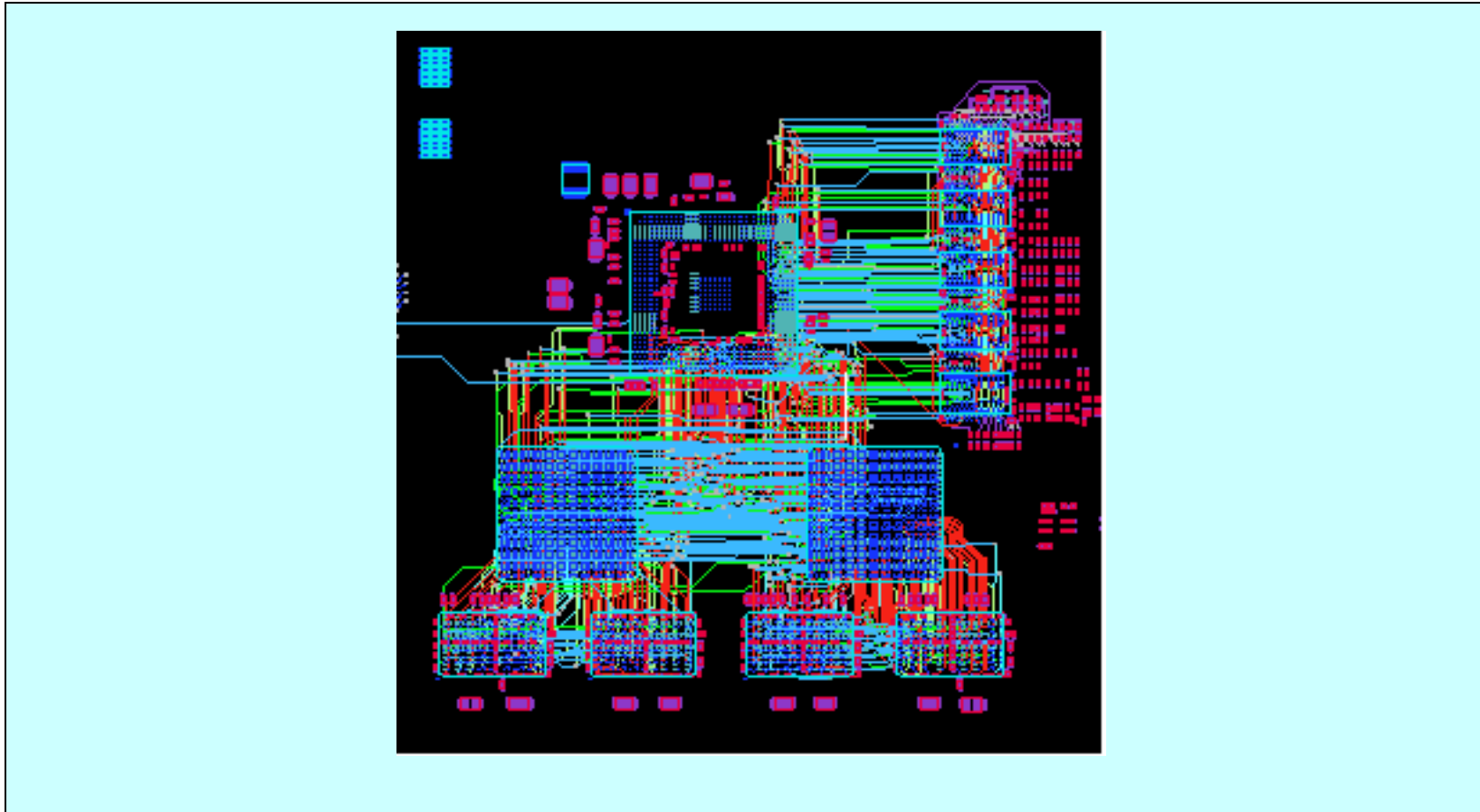


Slew Rates

- v **Interface Chip: Range 3 to 8 ns/V**



Layout and Routing

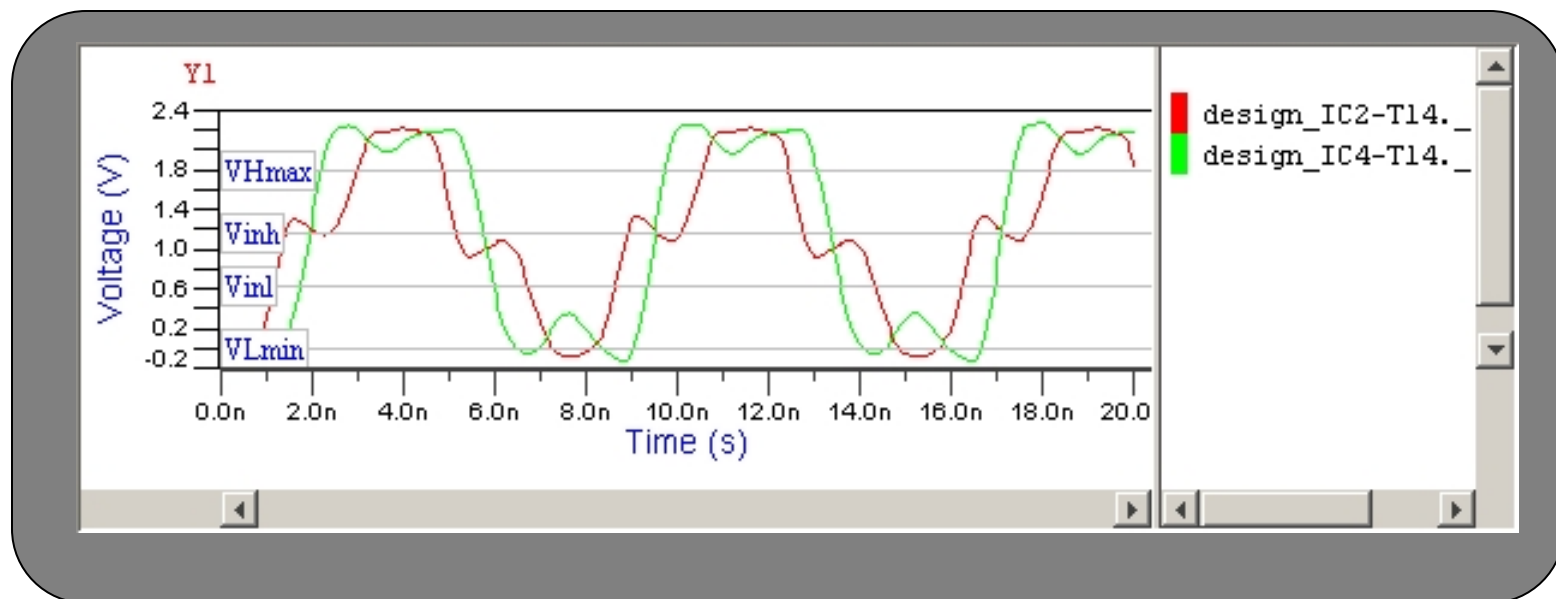


Board Layout and Routing

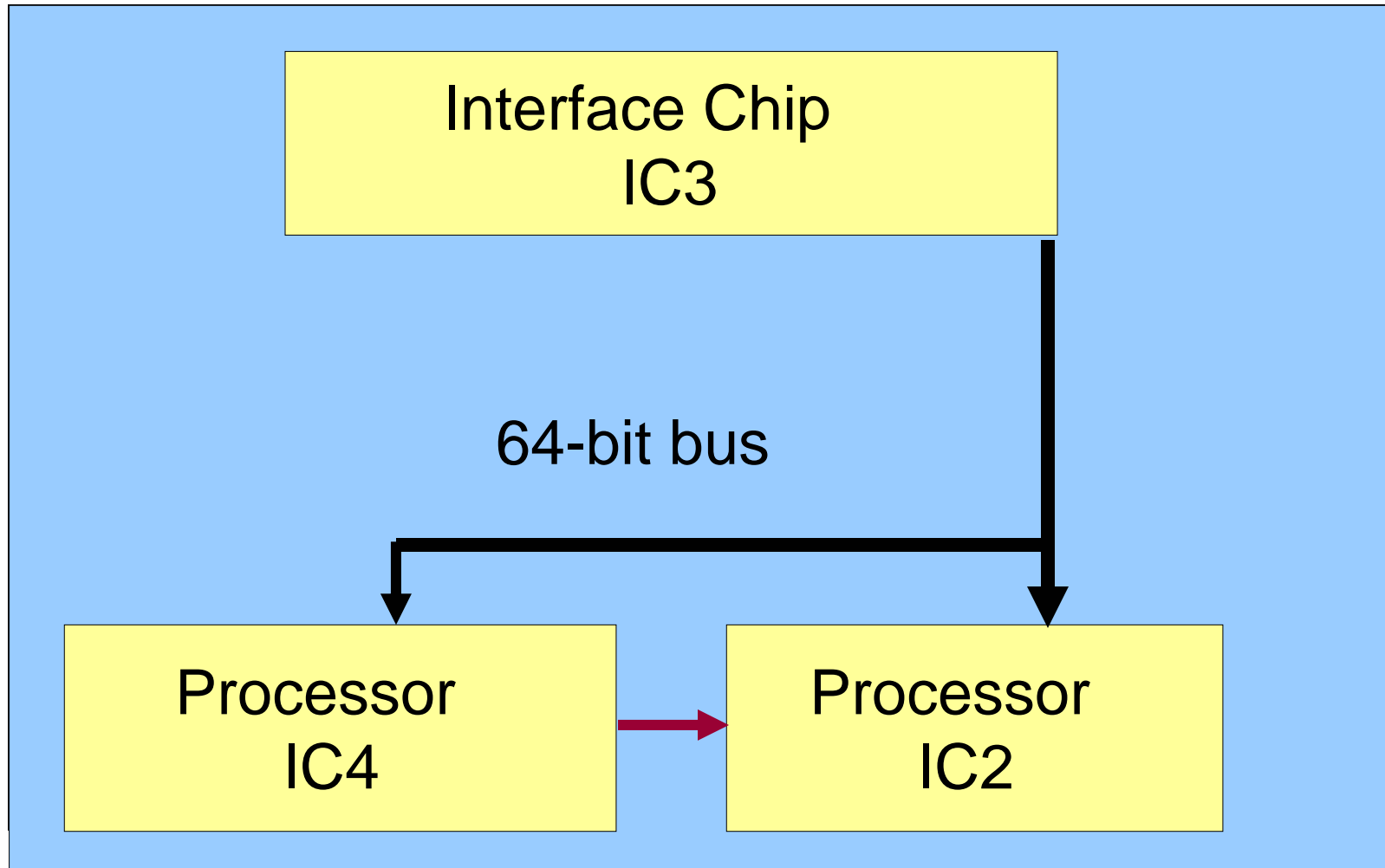
- ✓ **All traces have 50Ω characteristic impedance**
- ✓ **Average trace length 5.5 inches**
- ✓ **Routing topology is daisy chain**
 - **IC3 to IC2 then IC2 to IC4**
 - **Balanced routing takes up too many routing resources**

Un-terminated Bus Analysis

- v **IC3 drives IC2 and IC4**
 - **IC4 trace is acceptable**
 - **IC2 has non-monotonic dip near the high threshold**



IC3 drives IC2 and IC4



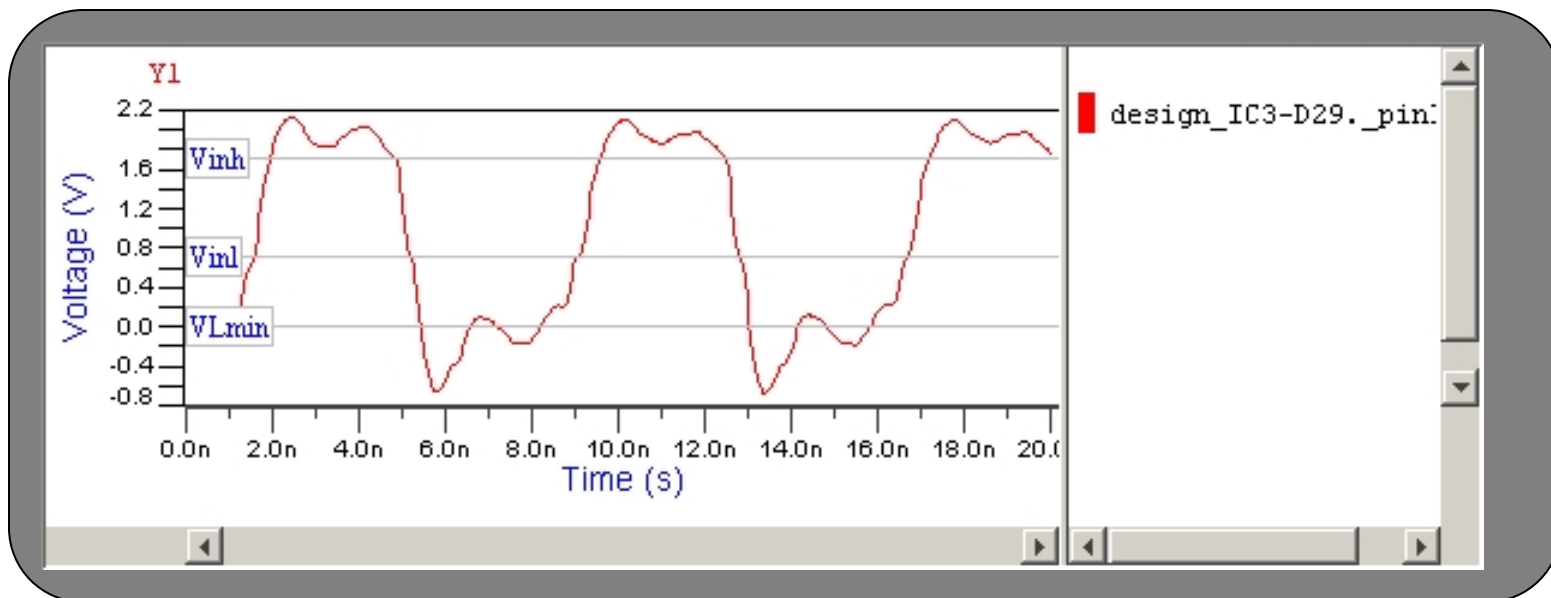
 Launched Waveform

 Reflected Waveform

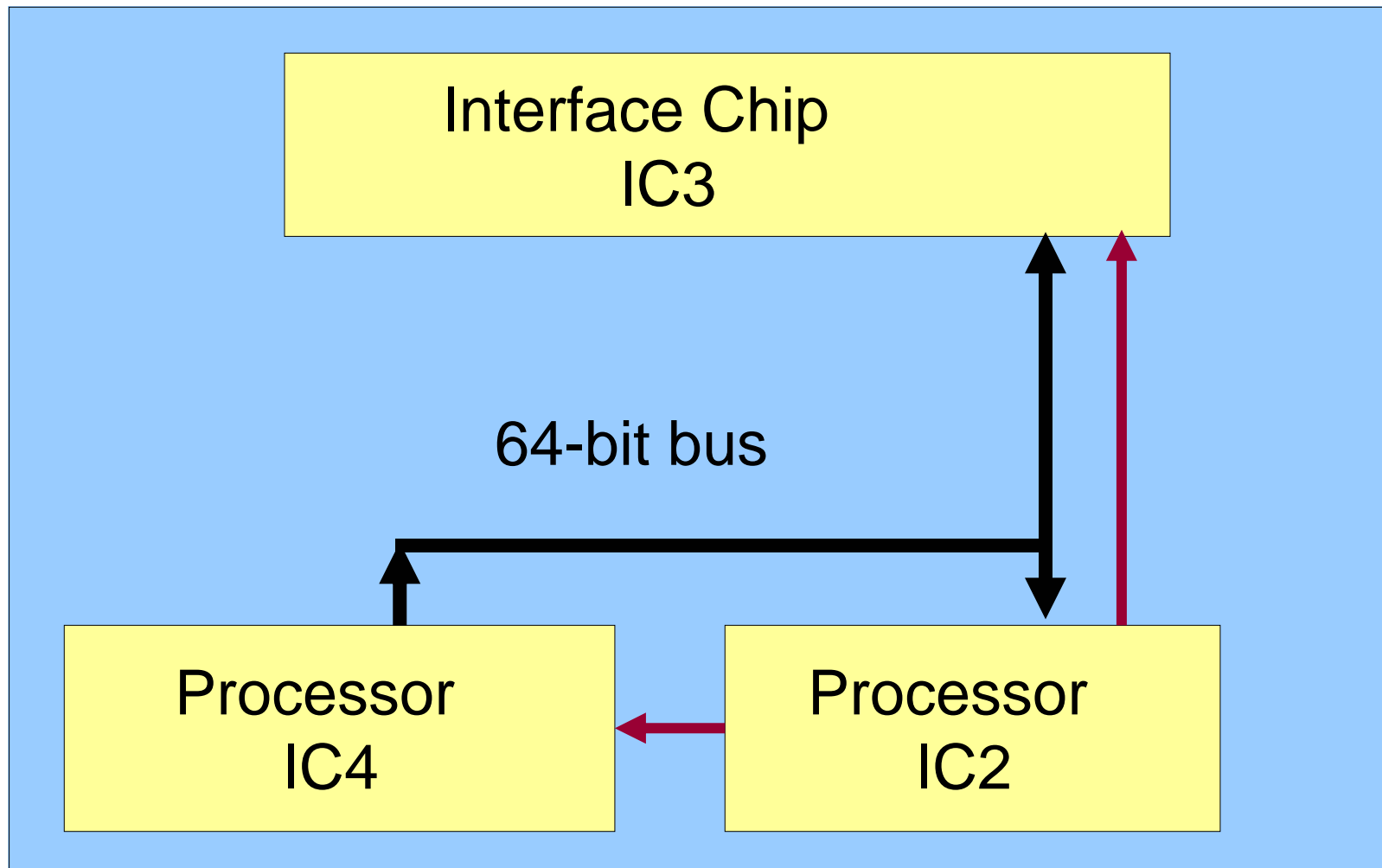


Un-terminated Bus Analysis (Contd.)

- v IC4 drives IC3
 - Undershoot is undesirable, though acceptable



IC4 drives IC3



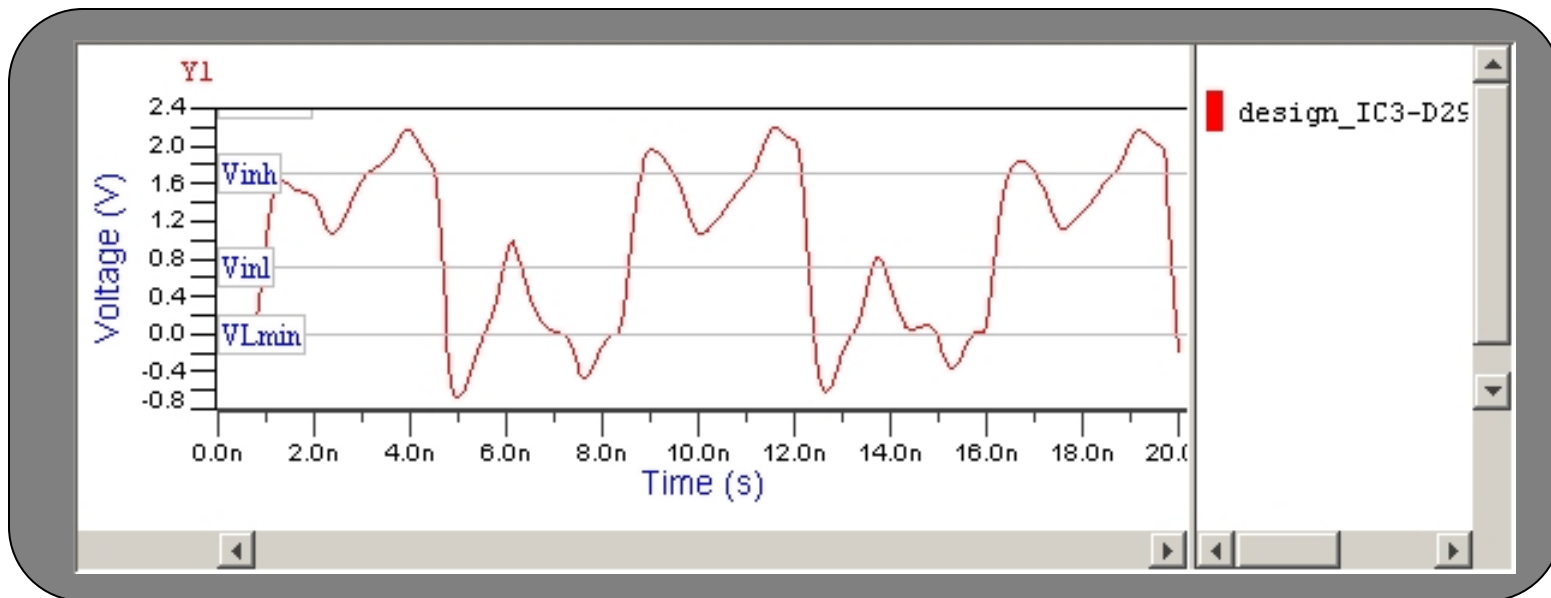
 Launched Waveform

 Reflected Waveform

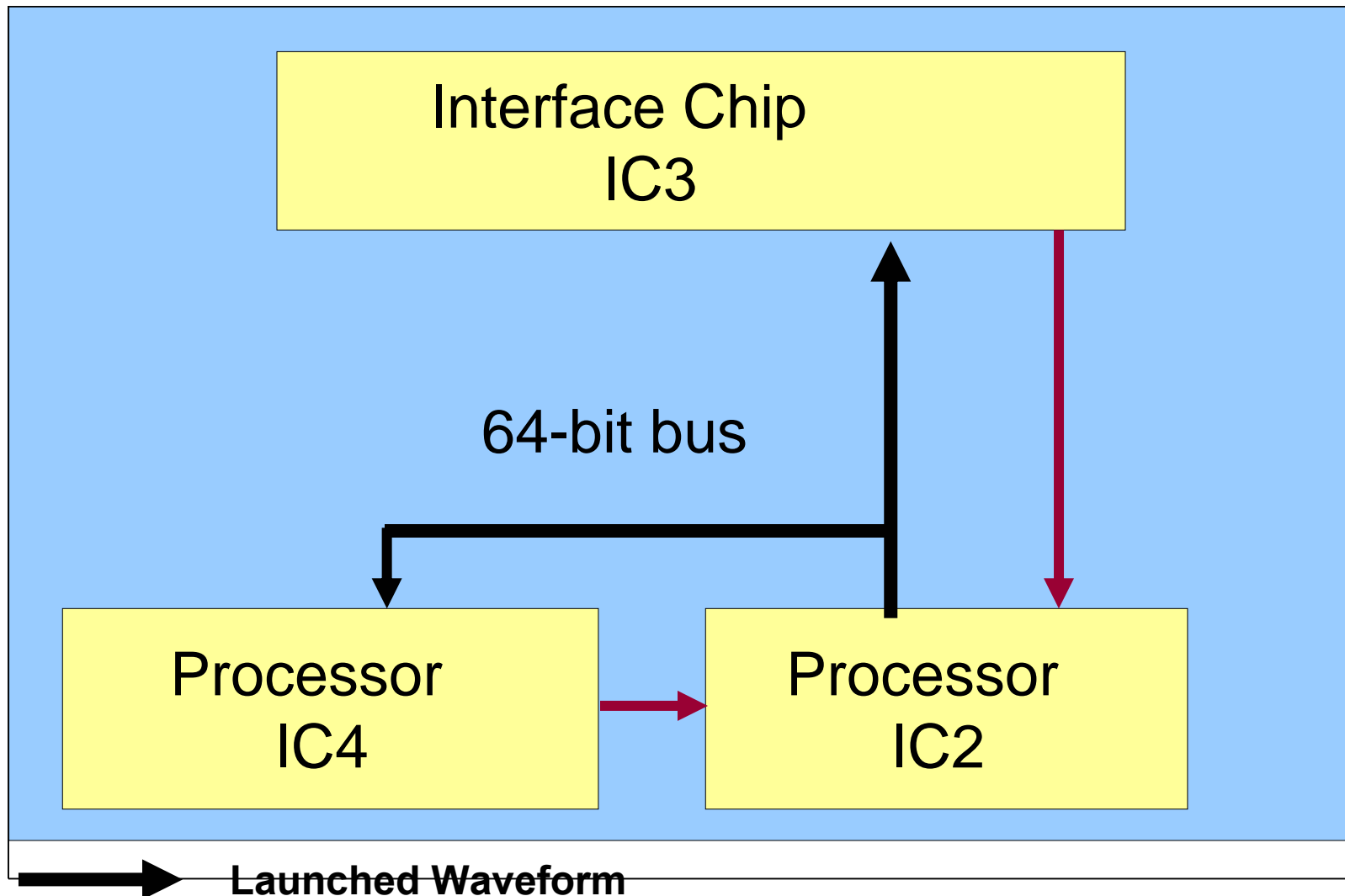


Un-terminated Bus Analysis (Contd.)

- v **IC2 drives IC3.**
 - **Signal integrity problem in both high and low transition region.**



IC2 drives IC3



Termination Will Solve the Problem

- ✓ **Series resistors near drivers will match the driver to the transmission line.**
- ✓ **Resistor tied to power or ground with the value of the transmission line placed at the receiver will match the receiver to the transmission line.**
- ✓ **If each node is terminated, 384 resistors need to be placed!**
- ✓ **Desired result is one termination resistor per data line.**



Termination Optimization

- v **ICX can determine the termination. Described in chapter 10 of the ICX user's guide.**

— Steps.

- v **Un-route trace.**
- v **Set-up noise rules.**
- v **Set-up termination rules.**
- v **Run signal optimization.**
- v **Check results.**

Set-up of Noise Rules Spreadsheet

- Rules were relaxed to allow optimization.

	<i>Electrical Net</i>	Crosstalk (mV)	Undershoot (mV)	Overshoot (mV)	Ringback Low Margin (mV)	Ringback High Margin (mV)	Monotonicity Required	Characteristic Impedance (ohms)
			200.00	200.00			no	50.00
			300.00	450.00			no	50.00
	/D(0)							
	/D(1)							
	/D(2)							
	/D(3)							
	/D(4)							
	/D(5)							
	/D(6)							
	/D(7)							
	/D(8)							

Set-up Termination Rule Spreadsheet

File Edit Report Options Help

Classes Electrical Topology Manufacturing

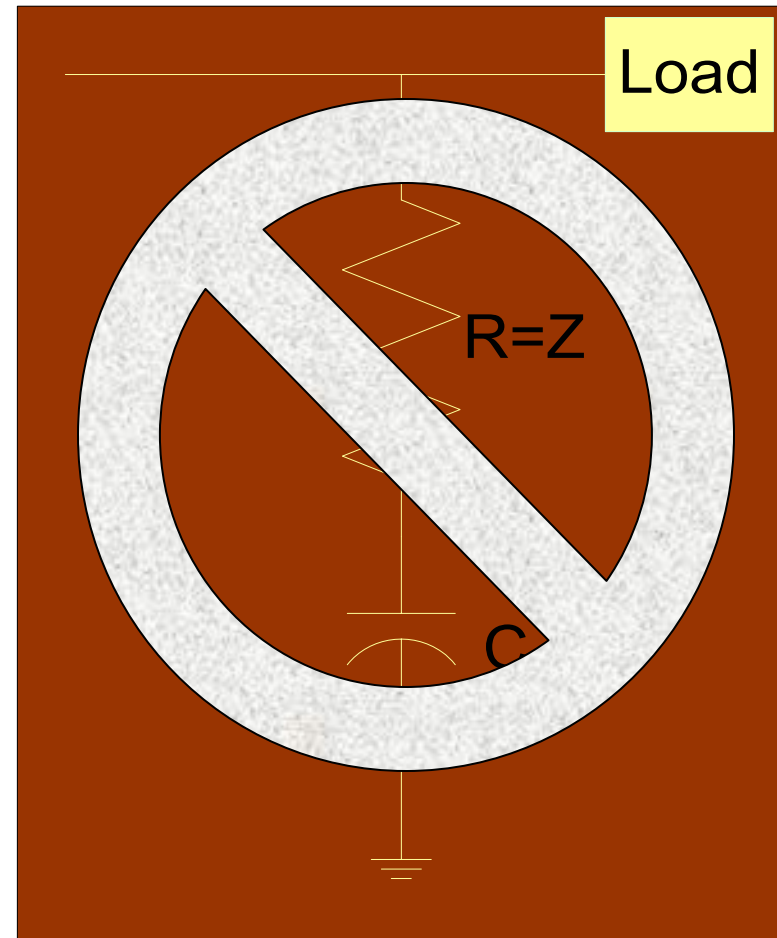
Noise Timing Bus Timing Paths Integrity

Electrical Net	Optimization Methods	Prioritized Optimization Technique	Values
/D(0)			
/D(1)	Termination	RSeries	a_RSeries_15 a_RSeries_30
		Pullup	a_Pullup_50_+2.5V a_Pullup_50_+1.8V a_Pullup_100_+2.5V
		Pulldown	a_Pulldown_50_GRD a_Pulldown_75_GRD
/D(2)			
/D(3)			
/D(4)			

Apply Reset Find...

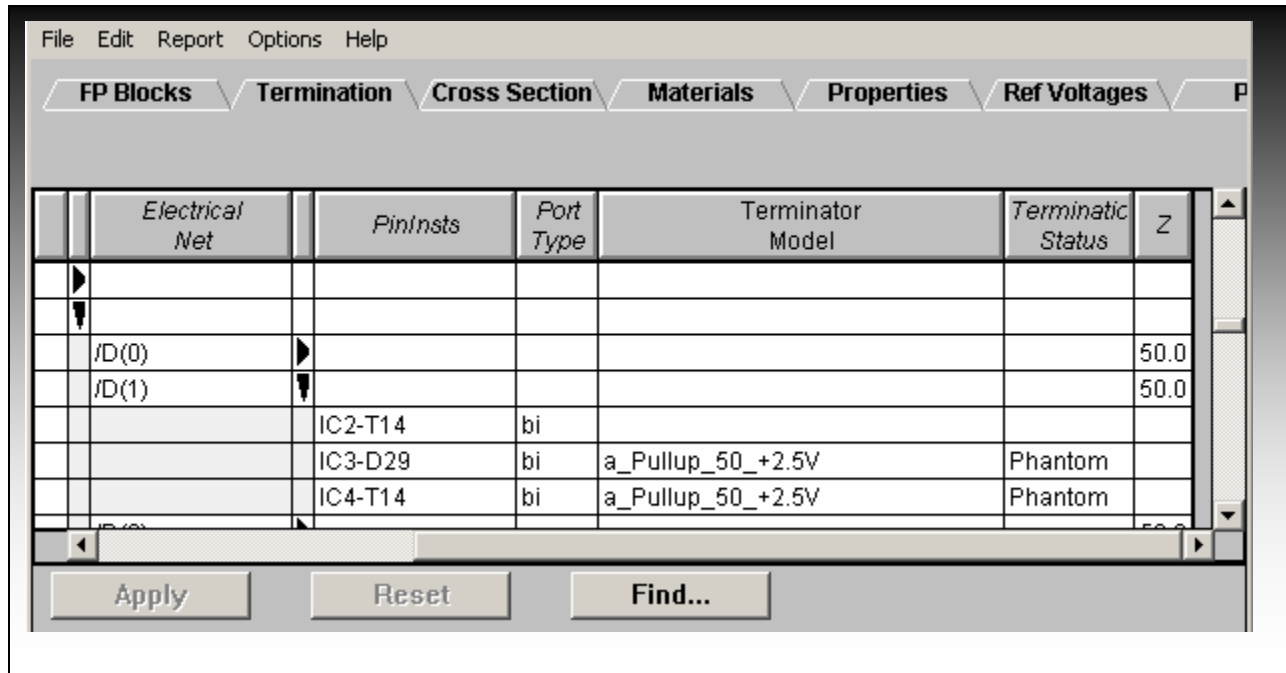
AC Terminations

- v During transitions the capacitor shorts resistor to ground. During steady state operation the resistor is an open circuit.



Optimization Results

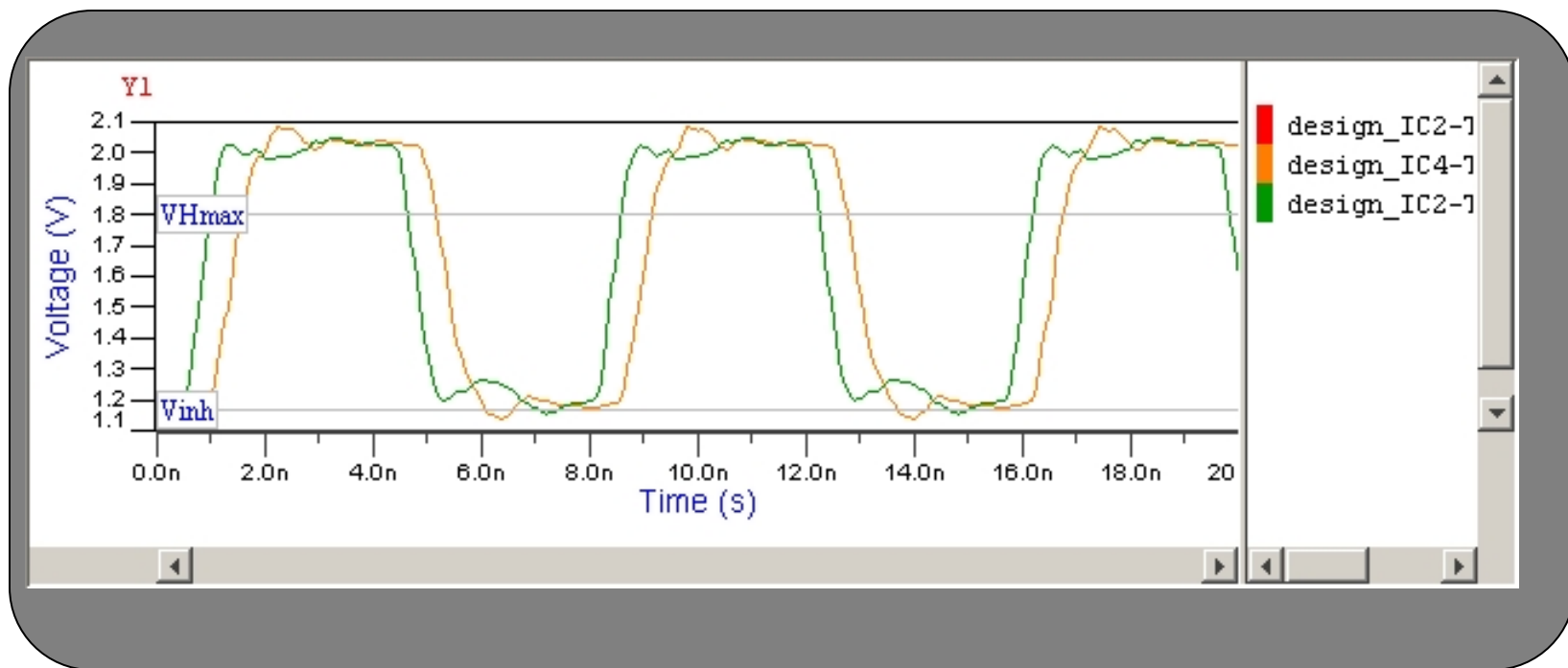
- ✓ The optimization results indicate that 50Ω pullup resistors should be placed at IC3 and IC4.



Electrical Net	PinInsts	Port Type	Terminator Model	Termination Status	Z
/D(0)					50.0
/D(1)					50.0
	IC2-T14	bi			
	IC3-D29	bi	a_Pullup_50_+2.5V	Phantom	
	IC4-T14	bi	a_Pullup_50_+2.5V	Phantom	

Problem With Optimization Results

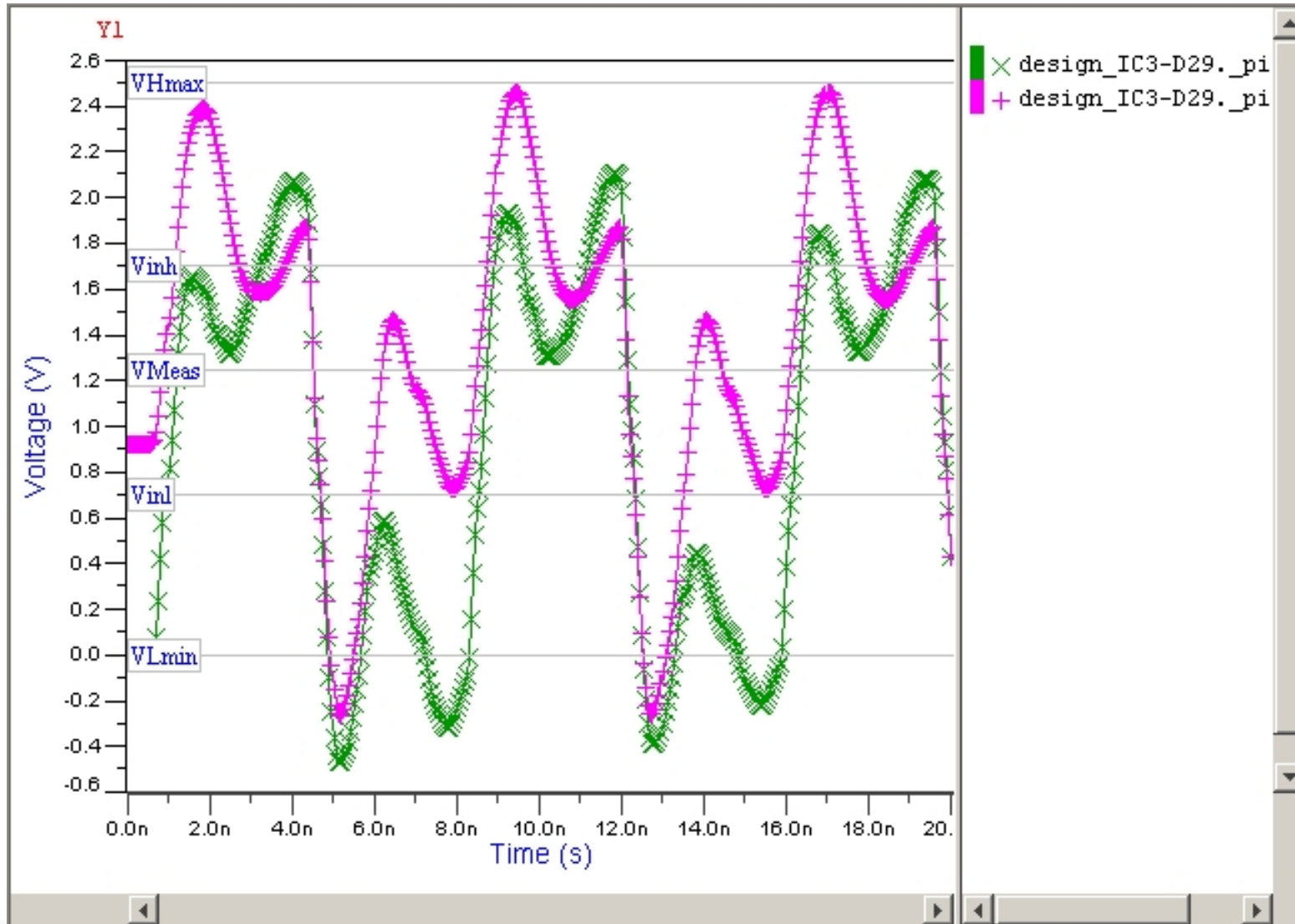
- Current is too high! 40 mA for a 1V swing.
- Signal will never go low.



Engineering and ICX Solve the Problem

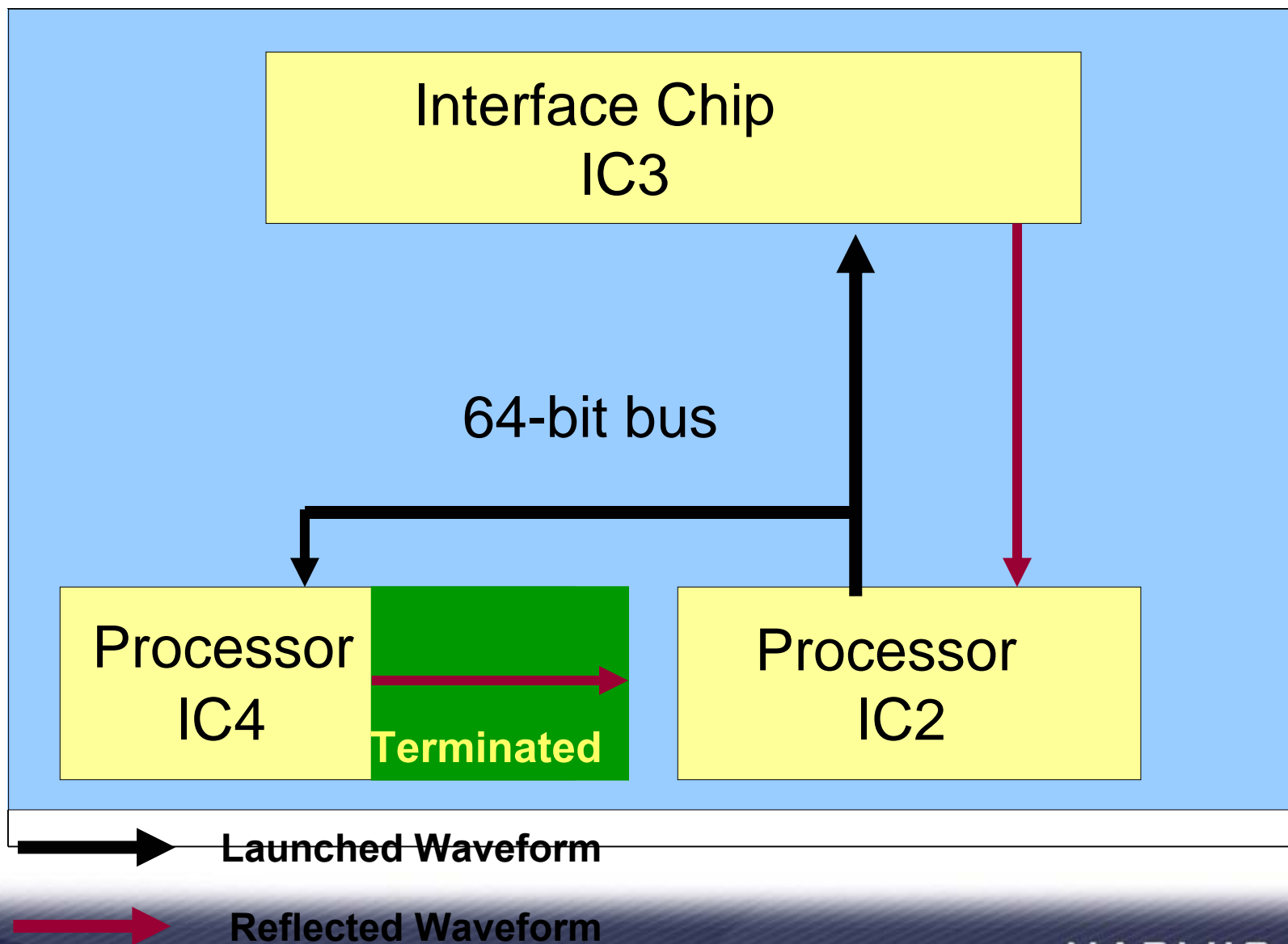
- ✓ **The only area where termination resistors can be placed is near IC4.**
- ✓ **The desired solution is only to use one resistor.**
- ✓ **Removed the termination resistor at IC3 and kept the termination resistor at IC4.**

Terminated Vs. Un-terminated Results



x marker is terminated. + marker is un-terminated.

IC2 drives IC3 with termination



Trade-offs in Signal Quality

- v **Improvements with one termination.**
 - Low voltage stays low. High voltage has improved, but the waveform still crosses the high threshold.
 - High voltage has a smooth rise time.
 - Best trade-off between signal quality, rise time noise immunity, power and component placement.
- v **Regardless: 4 nanoseconds are needed for signal settling time.**

Summary and Conclusions

- ✓ **Microprocessor data busses pose a signal integrity problem.**
- ✓ **ICX can be used to find the termination scheme.**
- ✓ **The feasibility of the termination scheme must be evaluated for noise immunity, timing and placement feasibility.**

Summary and Conclusions (Contd.)

- ✓ **There is a trade-off between the optimal signal integrity solution and the practical realizable circuit.**
- ✓ **ICX combined with engineering expertise can properly solve high-speed microprocessor bus signal integrity problems.**

Questions?