Microprocessor Data Bus Signal Integrity Problems

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1. Microprocessor Data Buses

Microprocessor data buses are a signal integrity challenge. System configurations have non-homogenous devices manufactured on different processes all connected to the same bus. While each of these devices is characterized and approved to work at the specified bus voltages, due to device packaging, and driver slew rates there may be significant differences in input and output characteristics. What can be done when the differences in device processing and packaging create the situation that there does not seem to be a satisfactory solution to the signal integrity problem? Transmission line analysis and termination can be used to solve this type of a problem. There is a cost though, of increased rise time, lower noise immunity, higher power consumption and the addition of components in a congested area. An example of a technique utilizing termination features of ICX is discussed and a solution is presented for the signal integrity issues of a microprocessor data bus.

2. Transmission Lines

Signal traces on circuit boards can be considered a transmission line if the line length, in inches, is greater than the rise time of the signal, in nanoseconds. [1] The rise time of a signal is usually 10% of the period. The maximum un-terminated line length for a signal with a period of 100 MHz is 1 inch. A transmission line can be considered a circuit element that affects the signal transmission from one node to another node. The characteristic impedance of the transmission line is the key parameter in defining how the signal will interact with the transmission line. The characteristic impedance is a function of the conducting material, the insulating dielectric material and the spacing between the dielectric and the conductor. The most commonly used characteristic impedance in circuit boards is 50-Ohms. Traditionally 50-Ohms is a good compromise between performance and cost. [2]

Any impedance mismatch between the devices and the transmission line will result in signal reflections and a loss of signal at the receiving nodes. A parameter known as the reflection coefficient is a measure of how much of the source's signal will be reflected back to the source. Every node on the transmission line has its own reflection coefficient. If *R* is the impedance of the device attached to the transmission line and R_0 is the characteristic impedance of the transmission line, the equation for the reflection coefficient ρ is the following.[3]

$$\rho = \frac{\frac{R}{\mathrm{R}_0} - 1}{\frac{R}{R_0} + 1}$$

Equation 1: Reflection Coefficient

The technique of transmission line termination involves matching the characteristic impedance at the signal source and/or at the receiver. When the impedance of the devices is matched to that of the transmission line, the reflection coefficient becomes zero and all of the source's signal will be received without any reflected loss. ICX has the capacity to select from a combination of user specified termination types to achieve acceptable signal integrity results. [4]

3. Input Impedance

All CMOS devices have very large input impedance. The equations for the input impedance of a MOSFET are presented for reference in Appendix A. The assumption then is that all CMOS loads are the same, and only the parasitic effects contribute to load imbalance. The device package is the biggest contributor to the parasitic effect. Flip-chip packages have much less package capacitance resistance and inductance than wire-bonded chips.

4. Circuit Example

Figure 1 is a block diagram of a microprocessor system design. There are two microprocessors sharing a common bus. The bus is being controlled by an interface chip. The interface chip allows the microprocessor to access a shared memory and other devices. The bidirectional data lines of this bus present a signal integrity problem. The transmission line drivers and receivers of the microprocessor and the interface chip were of equal type and strength, and the package parasitic values which are shown for typical operating conditions in table 1 were not significantly different.

Parasitic	Processor	Interface Chip
Resistance	1.165Ω	0.486Ω
Capacitance	3.79pF	4.222pF
Inductance	6.118nH	4.222nH

Table 1: Comparison of Package Parasitic Parameters

There was a significant difference though in the slew rates of the output drivers of each device, which was determined from the data in the Ibis models. The processor had a slew rate of 2 Volts per nanoseconds and interface chip had a slew rate of 4 Volts per nanosecond. This created an unbalanced system.

All of the signal traces were specified as having a characteristic impedance of 50 Ohms. The bus requirement is to operate at a frequency of 133 MHz. The ranges of valid bus transactions are from the interface chip to the processors and from each individual processor to the interface chip. Transfers from processor to processor will never occur. This limits the analysis cases.

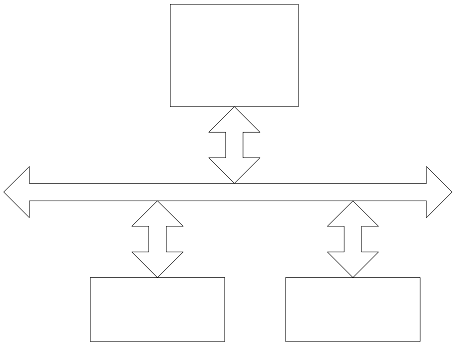

Figure 1: Microprocessor system

5. Board Layout

The board layout and initial routing of the data bus is shown in figure 2. The signal routing could not solve this category of problem. All of the traces were already of controlled impedance. A balanced routing topology would have two traces, from IC3 to IC2 and from IC3 to IC4, however this would use up the available routing resources. The only available routing topology was a daisy chain. This put the devices in a series configuration. The connection order was from IC3 to IC2 and then from IC2 to IC4. The average trace length was about 5.5 inches. The bus clock is 133 MHz; therefore the length is greater than signal rise time, which is 10% of the clock period, or 0.75 inches.

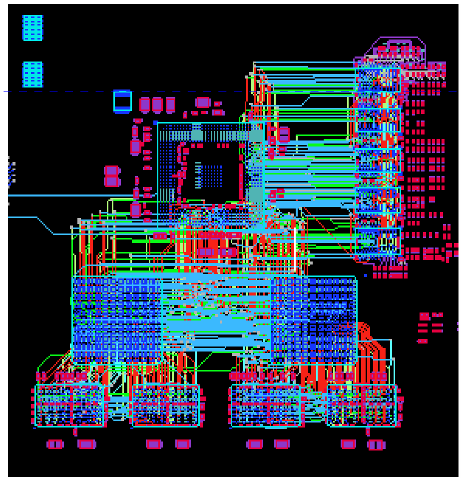

Figure 2: Layout and Initial Routing of Microprocessor System

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6. Initial Analysis of Un-terminated Bus

The simulations showed that the device in the middle of the trace IC2 showed the most problems. Signals propagating from IC3 to IC2 and IC4 need to pass through IC2. The load at IC2 became a point where signal was attenuated as well as a node where reflections seemed to collect. The initial waveform of what the signal characteristics for IC2 and IC4 when IC3 is driving the bus are shown in Figure 3. The waveform for IC4 appears acceptable. The waveform for IC2 has a non-monotonic characteristic near the high voltage threshold. This is a signal integrity problem. The voltage overshoot and undershoot will affect long-term reliability.

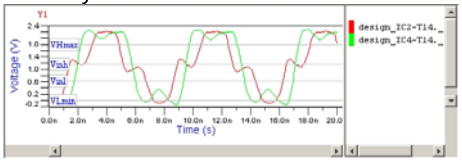

Figure 3: Un-terminated IC3 drives IC2 and IC4

The characteristics of the microprocessors driving the interface controller chip are also problematic. When IC4 is driving the bus the measured undershoot went below the ground rail for more than one nanosecond. This duration is not desirable. The waveform for this case is shown in figure 4.

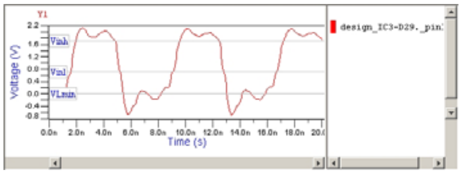

Figure 4: Un-terminated Case IC4 Drives IC3

The waveform of most troubling concern occurs when IC2 drives the bus. This waveform is shown in Figure 5. The measured undershoot goes below the ground rail for one nanosecond. There is also a signal bounce, which goes beyond the low voltage threshold for half a nanosecond. The high waveform has two peaks and a valley of amplitude. The voltage reaches the high voltage level, then dips below the threshold, and then rises above the threshold.

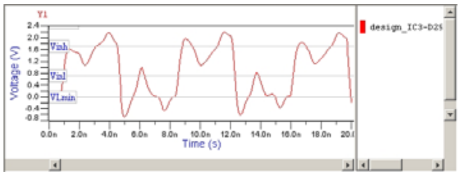

Figure 5: Un-terminated IC2 Drives IC3

7. Termination of the Transmission Line Will Solve the Problem

Without the capability to improve the routing, the best approach for the solution of the signal integrity problem presented is to terminate the transmission line. Series termination resistors may be placed near drivers to match the driver impedance to the transmission line. The effect will add rise time to the voltage waveform. Parallel terminations to power and ground may be added at each load to match the characteristic impedance of the net to the receiver. The board layout will not allow the insertion of all of these resistors. If at every node a series and parallel resistor are added, then 392 resistors need to be placed. Clearly, this was unreasonable. The best approach would be to terminate each data line with one or two resistors at the area left of IC4. There is some room available in that region for termination resistors. How can the choice of termination resistor and type be determined? Is there a way for ICX to determine the best termination resistor values and placement?

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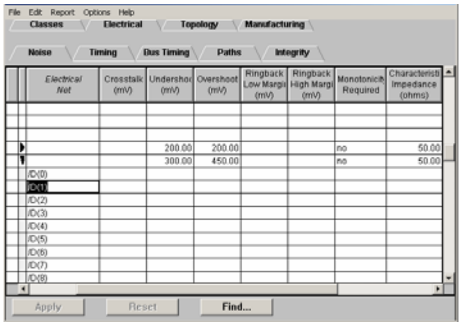
8. Signal Integrity Optimization Feature of ICX

ICX has signal integrity optimization. The ICX tool can chose between user specified termination types to determine the best combination and values of termination resistors that will solve the signal integrity problem. The user first sets up the noise requirements for the signals. The maximum overshoot and undershoot may be specified in the Rules, Noise spreadsheet. A user can tell ICX to use the termination optimization by selecting the termination optimization in the Rules, Electrical Optimization spreadsheet. The sheet allows a user to place a few types and values of termination resistor available. The user can select the node closest to the termination resistor. For analysis, phantom terminators are used. These phantom resistors are easily created in ICX. They may be created through a menu selection when one inputs the termination choices in the termination spreadsheet. When Signal Integrity optimization is performed, ICX will evaluate each one of the possible solutions. The best solution that meets the noise requirements will be displayed in the design data termination spreadsheet. The rest of this paper will illustrate the process and subsequent evaluation of the solution.

9. Signal Integrity Optimization Process

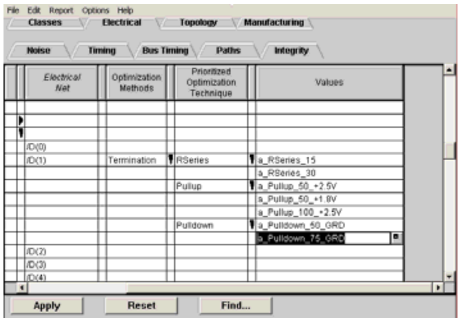
Figure 6 illustrates how the noise requirements were input for a data bit of the bus.



Electrical Net	Crosstalk (mV)	Undershoo (mV)	Overshoot (mV)	Ringback Low Margi (mV)	Ringback High Margi (mV)	Monotonicit Required	Characteristi Impedance (ohms)
		200.00	200.00			no	50.00
		300.00	450.00			no	50.00
/D(0)							
/D(1)							
/D(2)							
/D(3)							
/D(4)							
/D(5)							
/D(6)							
/D(7)							
/D(8)							

Figure 6: Noise Rules Spreadsheet

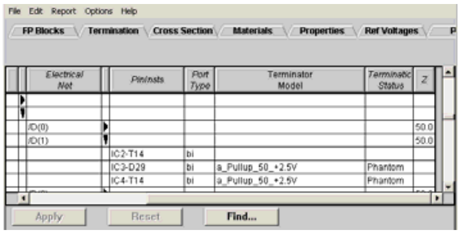
Figure 7 illustrates how the different types of phantom termination resistors were chosen and input to the spreadsheet. The desired result was one termination resistor per data line. The choice was limited to series, pull-up or pull-down terminations. The priority of these terminations was set in the spreadsheet. The order of the resistors sets the priorities.



Electrical Net	Optimization Methods	Prioritized Optimization Technique	Values
/D(0)			
/D(1)	Termination	RSeries	a_RSeries_15
			a_RSeries_30
		Pullup	a_Pullup_50_+2.5V
			a_Pullup_50_+1.8V
			a_Pullup_100_+2.5V
		Pulldown	a_Pulldown_50_GRD
			a_Pulldown_75_GRD
/D(2)			
/D(3)			
/D(4)			

Figure 7: Termination Rule Spreadsheet for Specifying Phantom Resistors

After the values were set, the net is selected, un-routed and a signal integrity optimization is run on the selected net. Following the optimization, the phantom resistor values appear in the termination spreadsheet. The results of the signal optimization are shown in figure 8. ICX has chosen to insert two phantom pull-up resistors of 50-ohms. The resistors should be placed near IC4 and IC3. These points are at the ends of the transmission line. The preferred method of the designer was a series termination. This preference was indicated by placing the series termination as first on the noise rules spreadsheet. However, ICX determined that the pull-up termination would give better results. Additionally, the voltage divider termination was not necessary as the pull-up termination yielded sufficient results. The Probe Net simulation is launched by the user to verify the results. The signal integrity engineer recommends the type value and placement of the termination resistors. The designer then incorporates these terminators into the design. Has the ICX tool performed the task of solving the signal integrity dilemma?



Electrical Net	PinInsts	Port Type	Terminator Model	Terminatio Status	Z
/D(0)					50.0
/D(1)					50.0
	IC2-T14	bi			
	IC3-D29	bi	a_Pullup_50_+2.5V	Phantom	
	IC4-T14	bi	a_Pullup_50_+2.5V	Phantom	

Figure 8: Design Data Spreadsheet with Phantom Resistors Inserted by the Signal Integrity Optimization

10. Probe Net Shows a Problem

The results indicated by the signal integrity optimization as shown in figure 8 calls for adding two pull-up resistors of 50-Ohms to 2.5V. These termination resistors are in parallel. The effective pull-up resistance is therefore only 25-Ohms. This will sink 40 mA of current for a one-volt swing. This is clearly beyond most drive and power requirements. The Probe Net simulation confirms this hypothesis. Figure 9 shows the simulation result for the double termination case, of IC3 driving IC2 and IC4. Notice that the voltage never goes below the high voltage level. The input buffers cannot sink all of the required current.

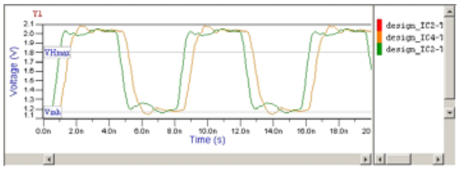


Figure 9: Signal Integrity Optimization Results

11. Engineering and ICX Solve the Dilemma

The desired result would be one termination resistor per signal in the design. Keeping this in mind, the decision was to remove the 50-Ohm phantom resistor that was placed at IC3. The only space for termination resistors is at IC4. The phantom resistor at IC3 was removed, the phantom resistor at IC4 was kept and the Probe net simulation was run. The results of the simulation are shown in figure 10.

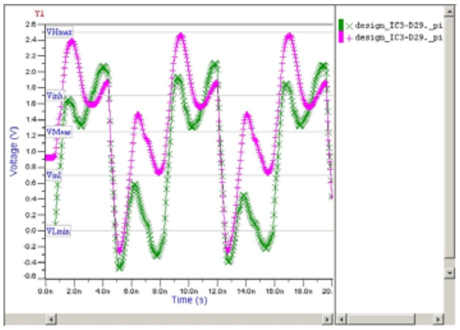


Figure 10: Pullup Terminated signal and Un-terminated Signal

The signal with the X marker has the pull-up termination resistor at IC4. The signal with the + marker is the original un-terminated waveform. The voltage waveform at the low voltage section has been significantly improved. The high voltage level has also been improved, by lowering the initial glitch of the rising waveform into the high voltage region. Regardless, for the high voltage level the signal required almost half a cycle (4 nS) to settle down. The reduction in the amplitude of the overshoot will reduce the noise generated by the signal. However, the signal rise time has increased. "It is always a good idea to use the slowest rise time that will meet the timing requirement." [5] Timing analysis confirmed that there were more than four nS of timing margin. The address lines switch at a rate of half the frequency, which is once every clock cycle.

12. Conclusion

As microprocessor data bus clock rates increase, transmission line terminations can escalate into a seemingly unsolvable problem. ICX has the capability to identify and fix signal integrity problems with the best termination scheme. The feasibility of the termination scheme must be evaluated for noise immunity, timing and placement feasibility. There is a trade-off between the optimal signal integrity solution and the practical realizable circuit. ICX combined with engineering expertise can properly solve high-speed microprocessor bus signal integrity problems.

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14. References

[1] Eric Bogatin, Signal Integrity Simplified (New Jersey, Prentice Hall, 2004) P. 299.
[2] Bogatin, P. 227.
[3] Herbert Taub, Donald Schilling, Digital Integrated Electronics (New York, McGraw-Hill, 1977) P.570.
[4] Mentor Graphics Corporation, ICX User's Guide, Software Version 3.2 (Oregon, 2003) Ch. 10.
[5] Micron Technology Inc., "Termination for Point-To-Point Systems, TN-46-06" (Idaho, 2001), P. 5.
[6] Taub and Schilling, P.259

Appendix A: MOSFET Input Impedance

The input impedance of a MOSFET is a function of the manufacturer's process. The equation for the input current to current of an n-channel MOSFET transistor I_{DS} is given by the equation.

$$I_{DS} = k(V_{GS} - V_{T})^2$$

Equation 2: Current in an N-Channel MOSFET

V_{GS} is the voltage from the gate to the source and V_T is the threshold voltage of the transistor. K is a constant that is defined by the chip process and geometry and is defined by the following equation.

$$k = \frac{\mu \varepsilon W}{2tL}$$

Equation 3: Process Specific Constant

Where μ = mobility of carriers in a channel (electrons in n-channel devices)
ε = Dielectric constant of oxide insulating layer
t = thickness of oxide under gate
W = Channel Width
L =Channel Length [6]

The input impedance of a device is the voltage swing divided by the current. If I_{DS} is the device current at the input MOSFET, there will be differences between the input impedance of parts manufactured with different processes. Not all CMOS inputs are the same, but the values are so large that they are not modeled.