

*Fix EMI Problems using Quiet Expert
Implementing an EMI Methodology*

**Mentor
Graphics®**

Agenda

- 1. Today's EMI Problem**
- 2. EMI Analysis Options**
- 3. Causes of EMI**
- 4. Design Rule Checks: Definition and Effectiveness**
- 5. Implementing an EMC Methodology**
- 6. Quiet Expert Tool Features**

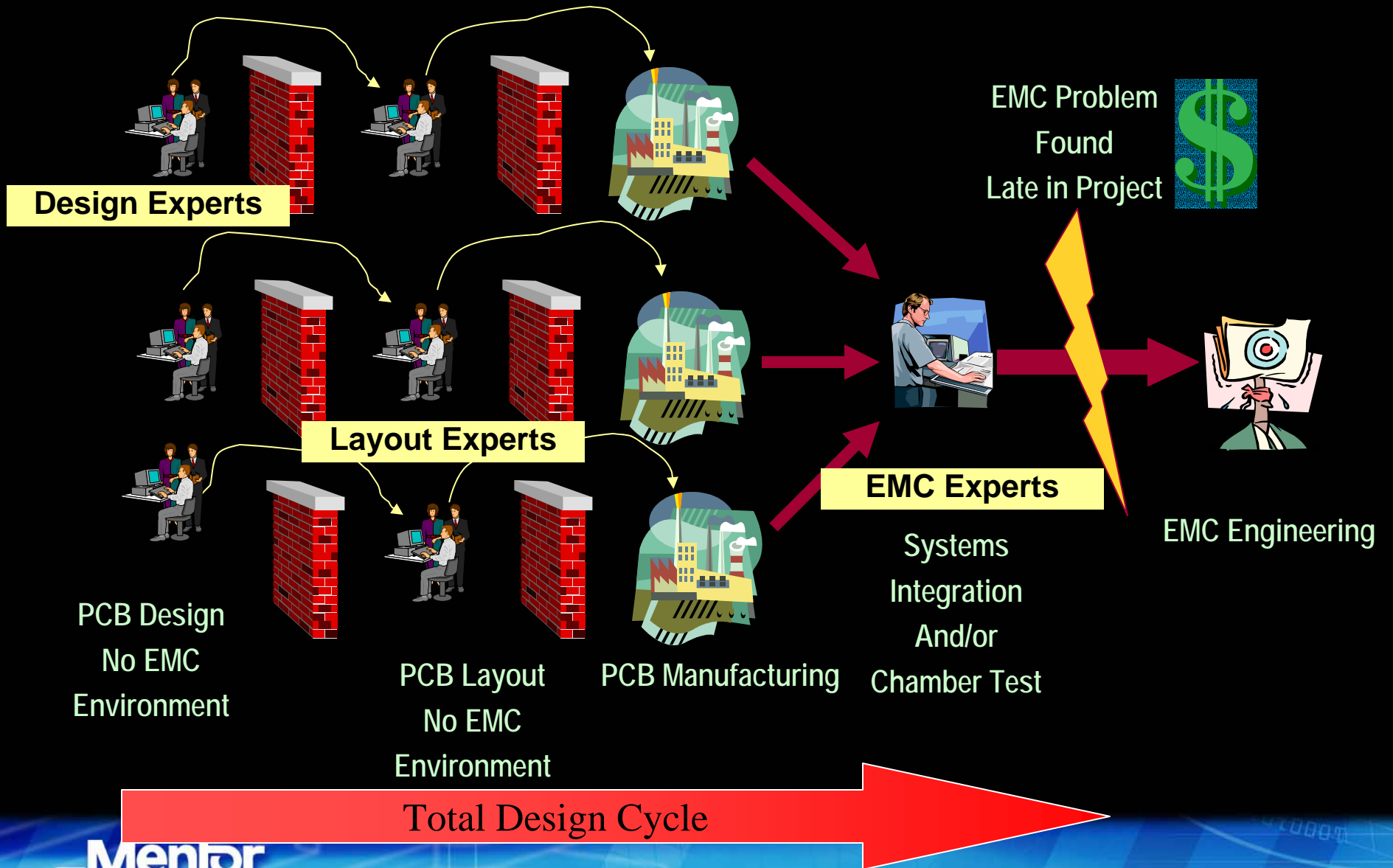
Goals for Today's Session

- ✓ **Provide non-EMC experts an understanding what causes EMC problems**
- ✓ **Why you DON'T need to know:**
 - **FDTD analysis**
 - **Far field vs. Near field**
 - **Horizontal Em measurements**
- ✓ **Understand good PCB layout practices with regards to EMC *and* signal integrity**
- ✓ **How to solve 75%-100% of your PCB EMC problems with a simple change in design flow.**
- ✓ **Understand good Design Rule Checks for EMC**

Chapter 1

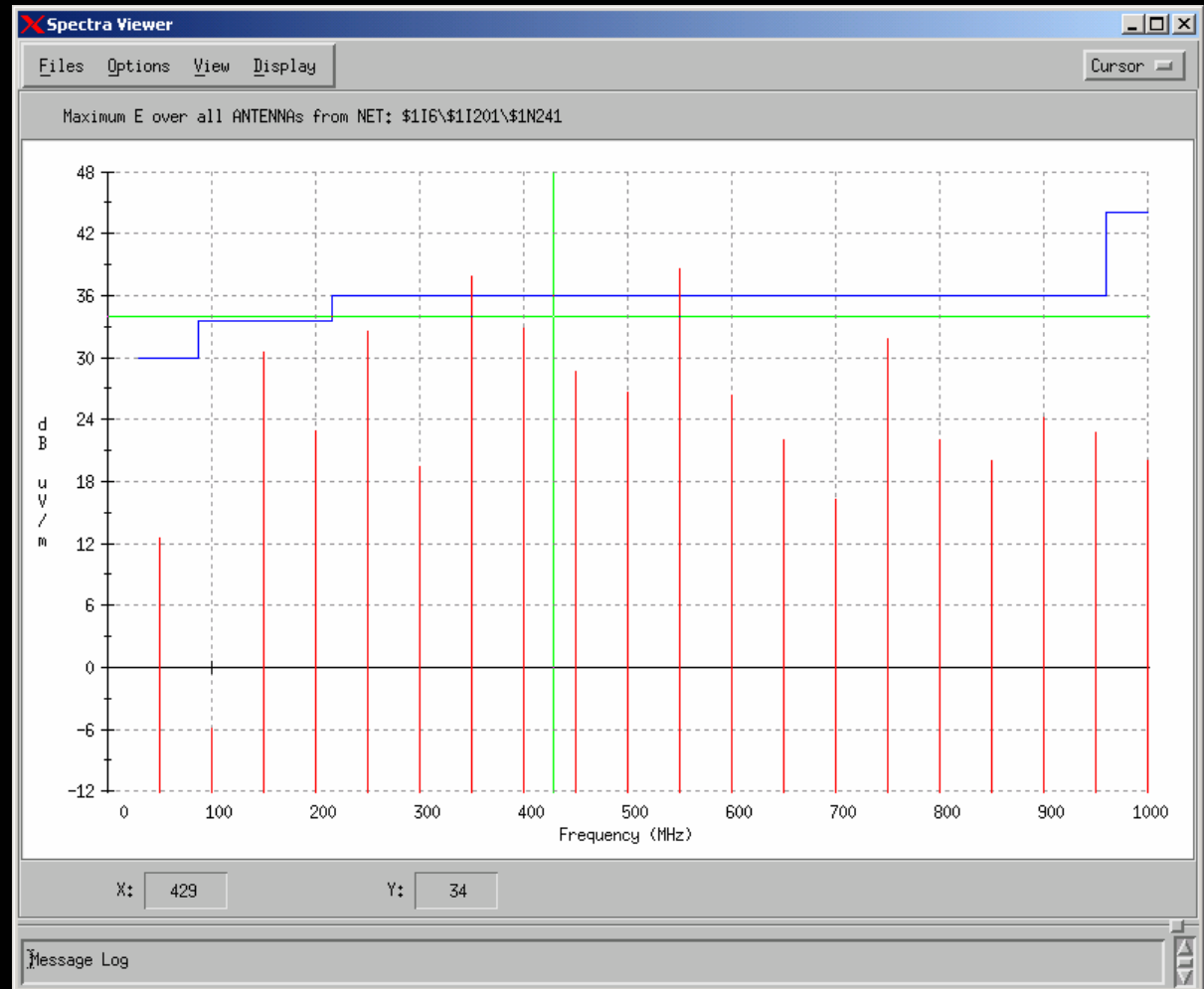
Today's EMI Problem

Customer Design Model

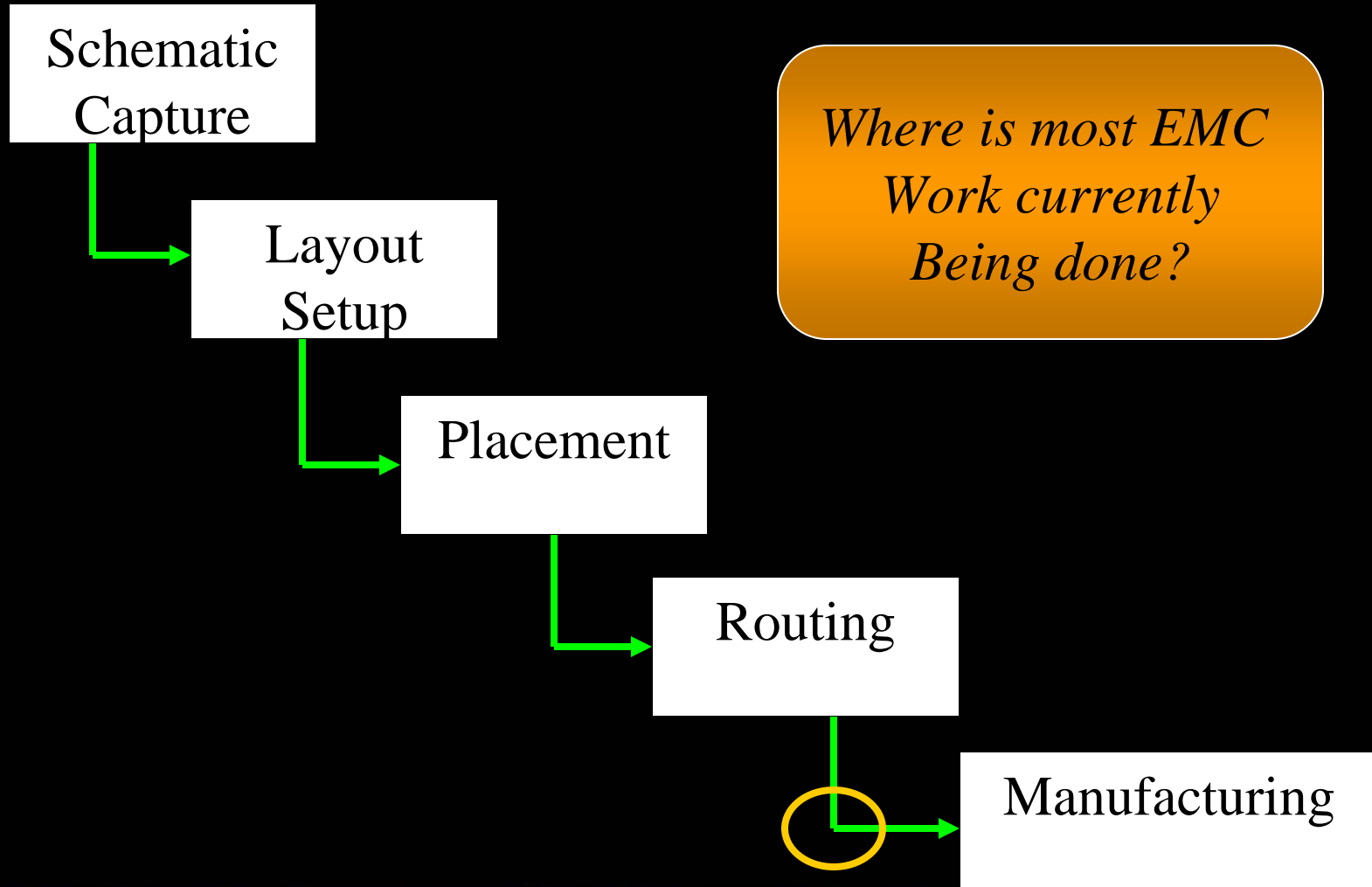


What does the EMC Expert see?

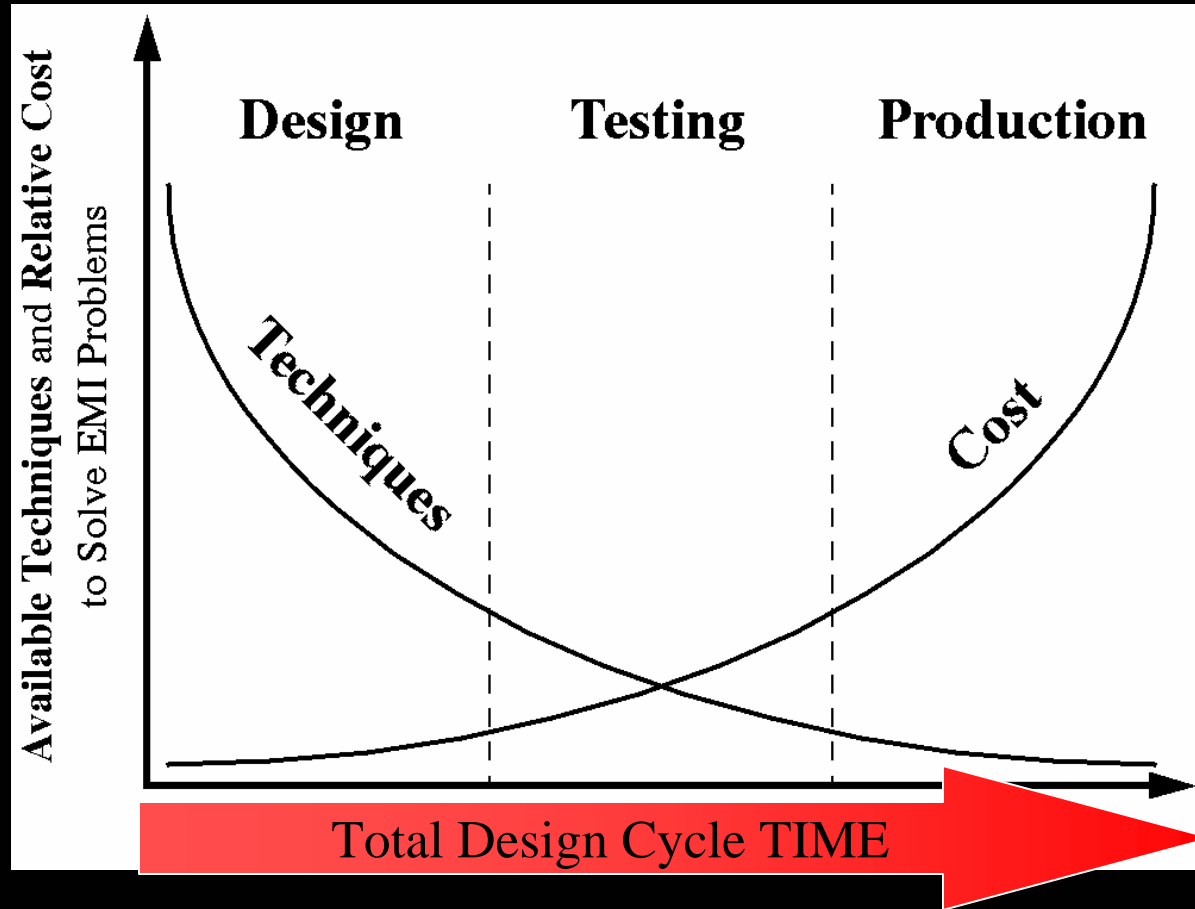
- v Does this pass FCC regulations?
- v What is the problem with this design?
- v **Reduction of 2dB passes!**



General Customer Design Flow



When do I fix EMI problems?



Ref: Ott, H., Noise Reduction Techniques in Electronic Systems, 2nd ed., John Wiley & Sons, 1988, p. 6.

Chapter 2

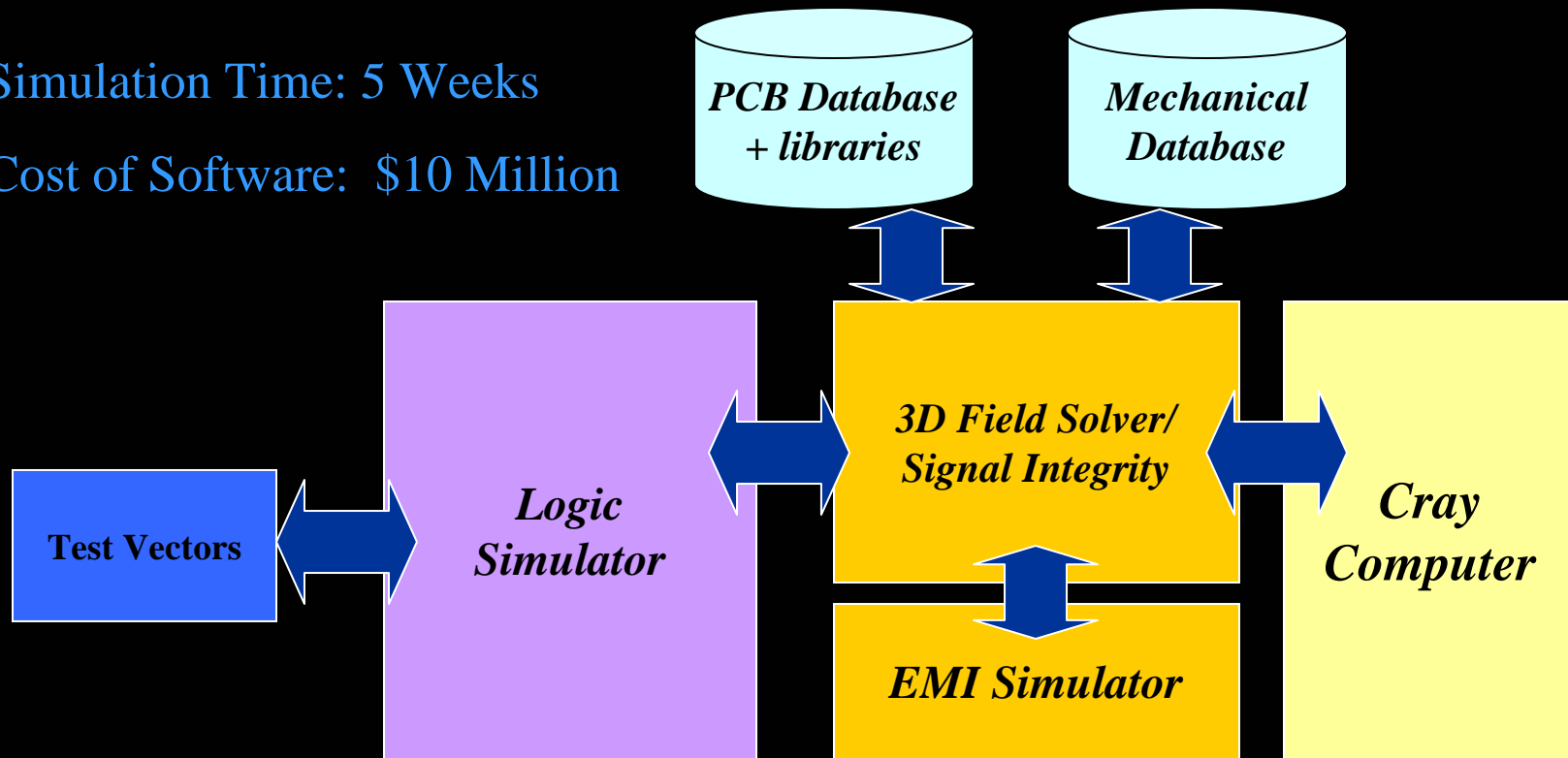
EMI Analysis Options

II. Analysis Options

- ✓ **Hope and Pray**
- ✓ **Simulation – Is it possible?**

Simulation Time: 5 Weeks

Cost of Software: \$10 Million



What about Signal Integrity?

- ✓ **Current SI simulation is considered to be good in the mV precision range.**
- ✓ **In EMI, uV noise on a good antenna can cause EMI Compliance failure**
- ✓ **Mechanisms that cause failure are not easy to identify or completely understood (much religious debate).**
- ✓ **Very small changes in input (e.g. duty cycle of a clock) can cause massive changes to measured EMI.**

Other Analysis Options

- ✓ **Hand Check Design Rules**
 - Works if you know your rules
 - Time Consuming
 - Prone to human error
 - Most companies have rules, but no automation or mechanism to implement and enforce them.
- ✓ **Confidence in DRCs critical to effective methodology**

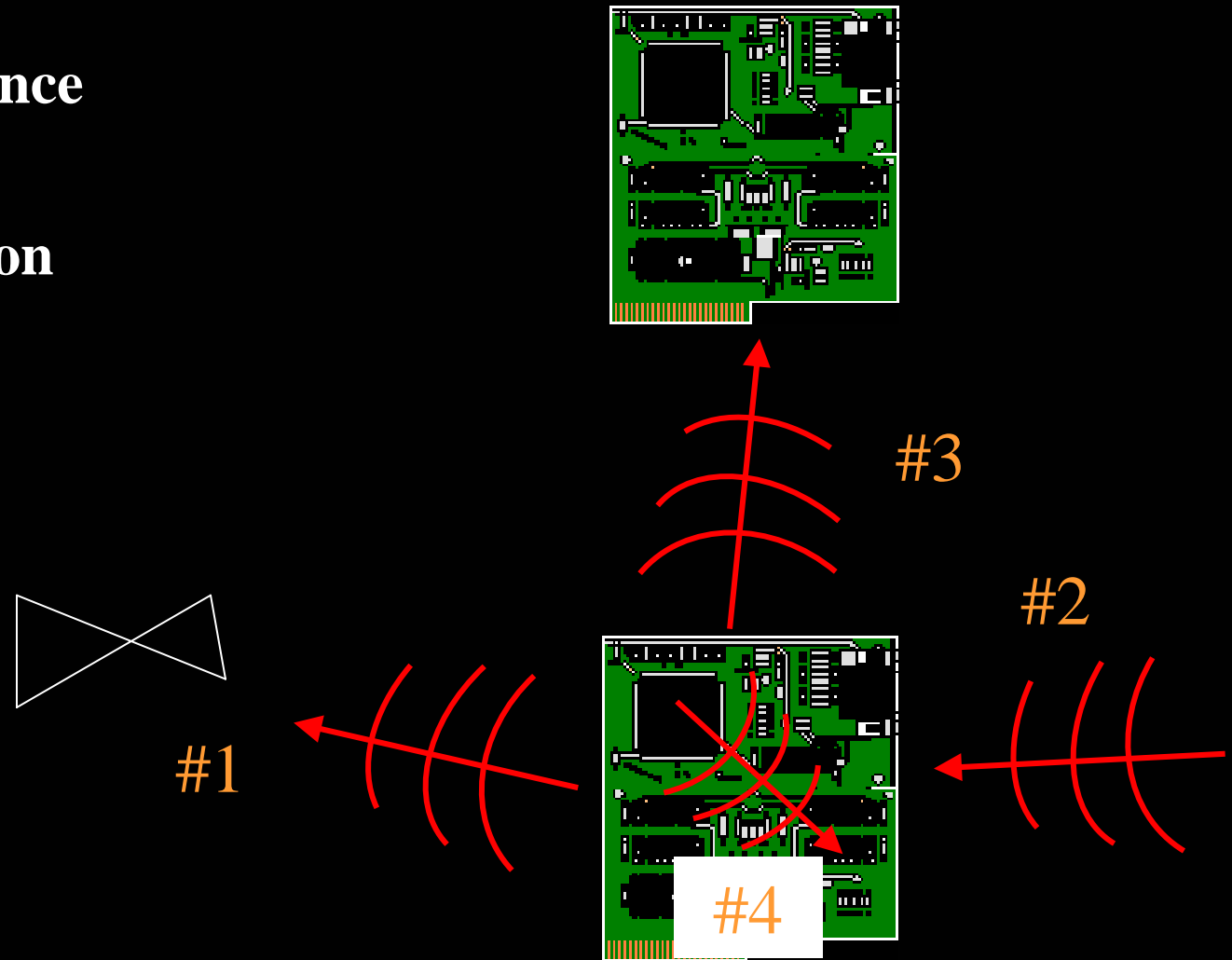
Chapter 3

Causes of EMC

Why the PCB should be your focus.

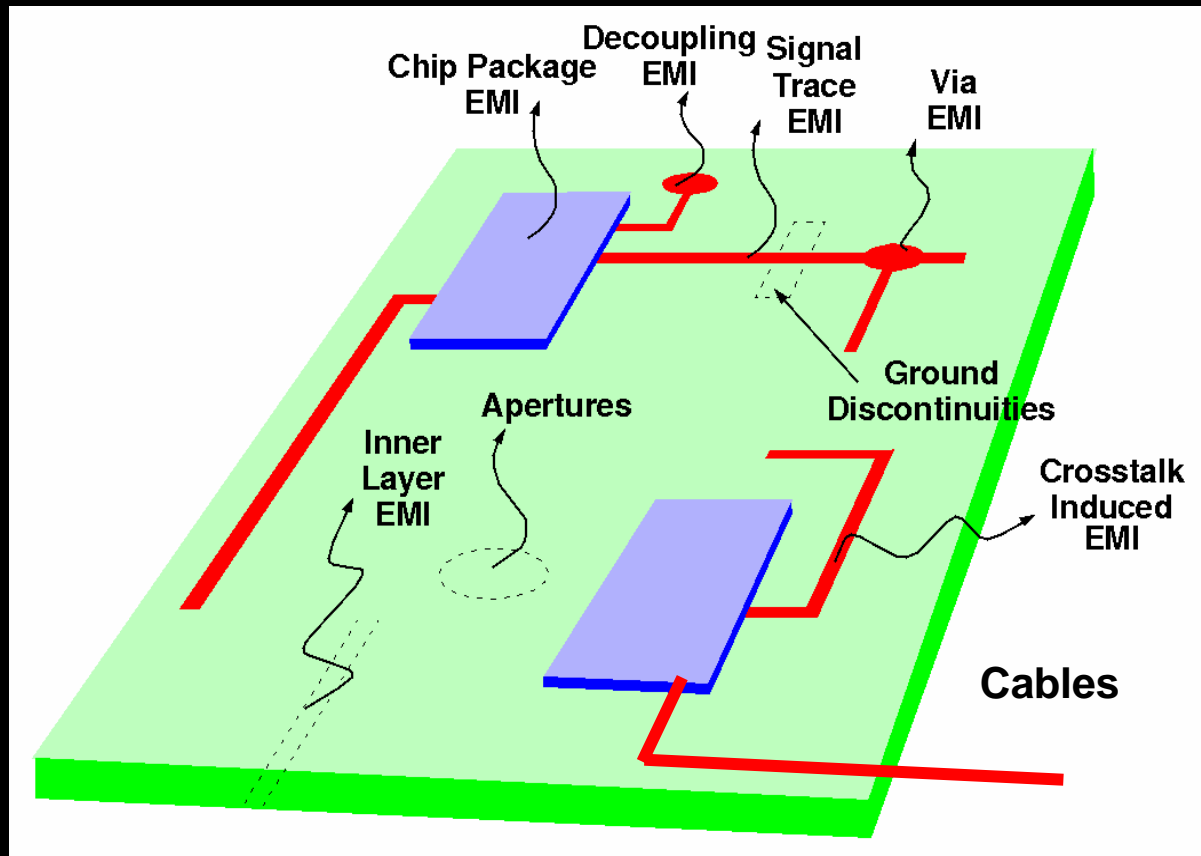
III. Top 4 Problems of EMC

1. EMC Compliance
2. Susceptibility
3. System Pollution
4. Self Pollution

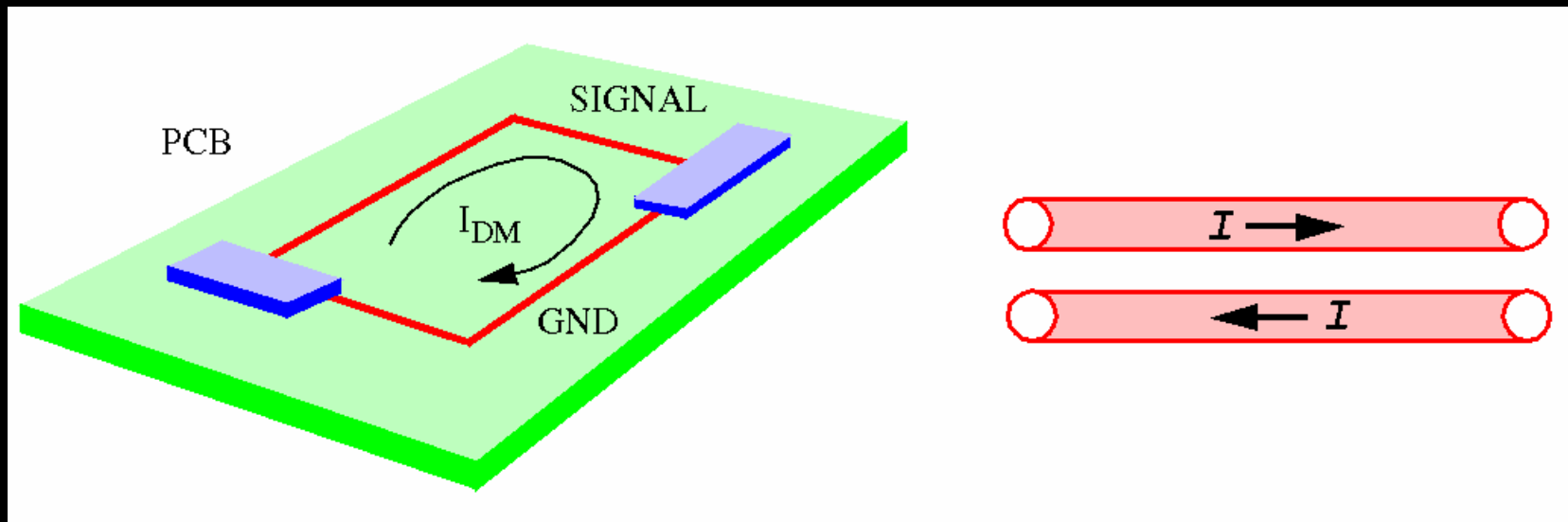


EMC Sources

- v Chips
- v Decoupling
- v Signal Trace
- v Via
- v Ground plane
- v Apertures
- v Cables
- v Crosstalk

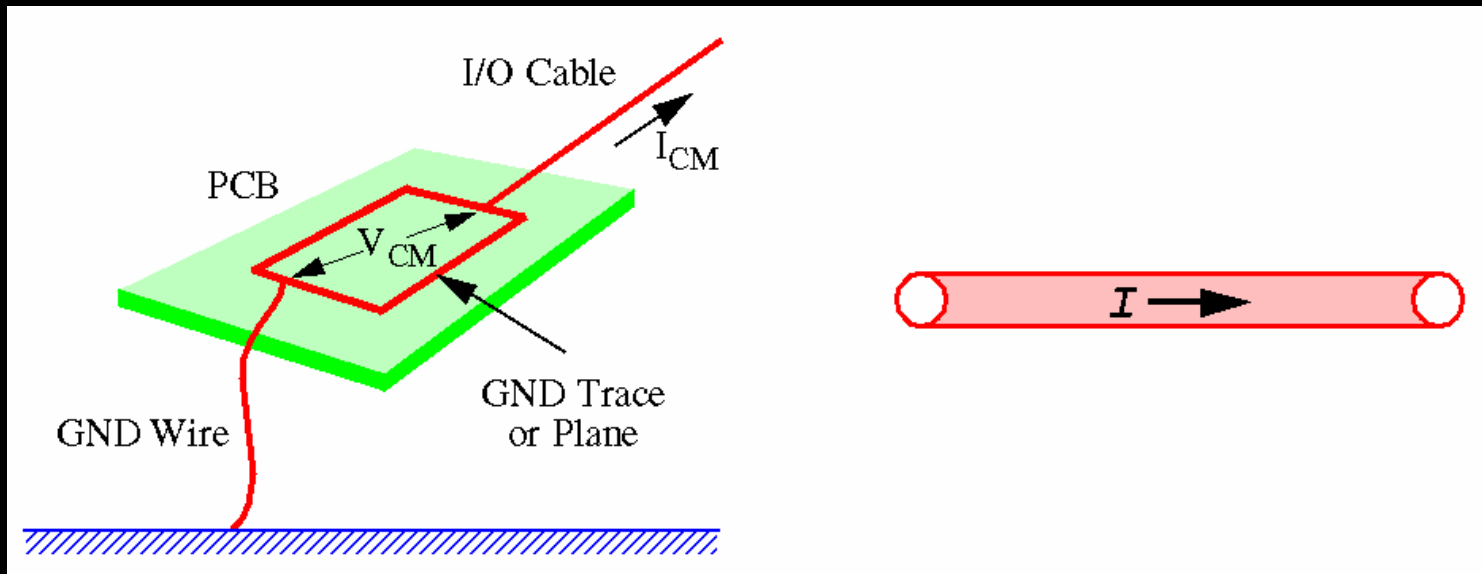


Differential Mode Radiation



- Modeled as Loop Antenna
- Examples:
 - trace-trace, trace-plane, chip package, ground slot, ...

Common Mode Radiation



- Modeled as Monopole Antenna
- Examples:
 - cable, cable shield, ...

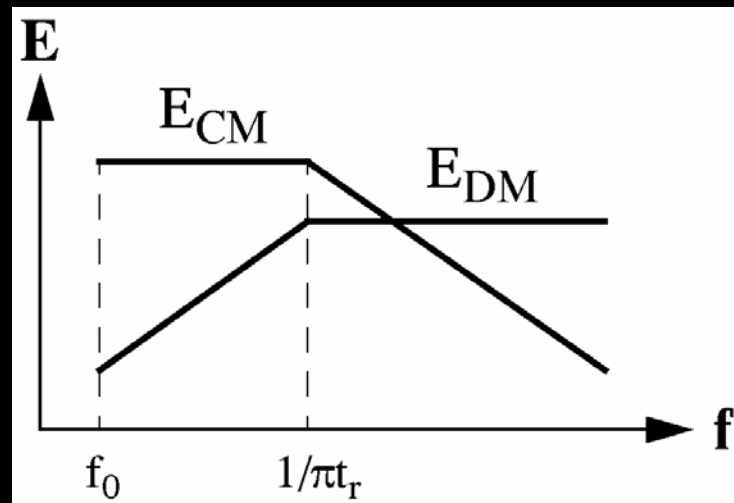
DM vs. CM Radiation

- DM radiation:

$$E_{DM} \propto \left(I_{DM} A \right) \frac{f^2}{r}$$

- CM radiation:

$$E_{CM} \propto \left(I_{CM} L \right) \frac{f}{r} \propto \left(I_{CM} L \lambda \right) \frac{f^2}{r}$$



DM and CM Control Techniques

- **DM emission control:**

- minimize I_{DM} and A

$$E_{DM} \propto \left(I_{DM} A \right) \frac{f^2}{r}$$

- **CM emission control:**

- minimize I_{DM} and A

$$E_{CM} \propto \left(I_{CM} L \right) \frac{f}{r} \propto \left(I_{CM} L \lambda \right) \frac{f^2}{r}$$

$$I_{CM} \propto \frac{V_{CM}}{Z_{CM}} \propto \frac{I_{DM} L_{CM}}{Z_{CM}} \propto \frac{I_{DM} A}{Z_{CM}}$$

- **Shielding is an effective but expensive solution for both DM and CM emission control**

- e.g. stripline, enclosure, cable shield.



Minimizing I_{DM} and A



- Use logic families that are no faster than necessary.
- Use the lowest clock frequency possible.
- Use the longest risetime possible for all pulse signals
- Keep all clock lines as short as possible.
- Tightly control the loop area of all high speed signals.
- Do not allow any traces to cross any gaps in the return plane.
- Provide a closely located return path for all critical signals.
- Provide at least one decoupling capacitor for each power pin.
- **Use Design Rule Checks (DRCs) to minimize area**

I_{DM}

A

Chapter 4

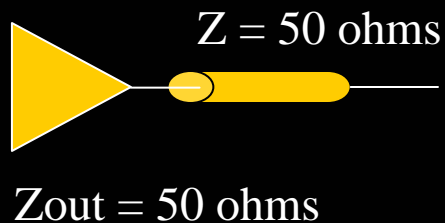
Design Rule Checks Definition and effectiveness

Definitions

- ✓ **Design Rule Check (DRC):** A ordinance or regulation that should be followed to insure proper operation of the design according to its specification.
- ✓ **Examples:**

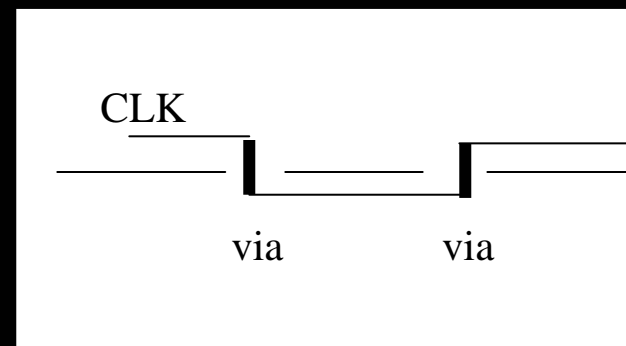
Signal Integrity

Match Impedance
with Driver

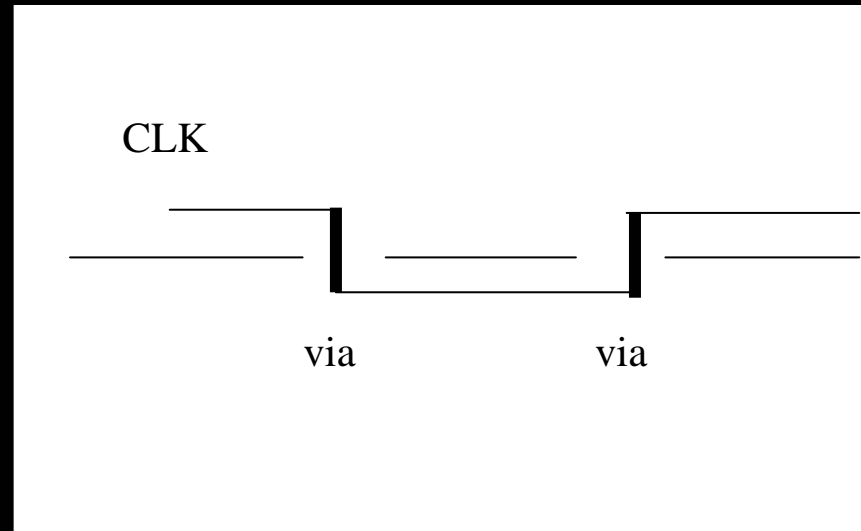


EMC

No more than 2 vias (layer changes) on a clock trace

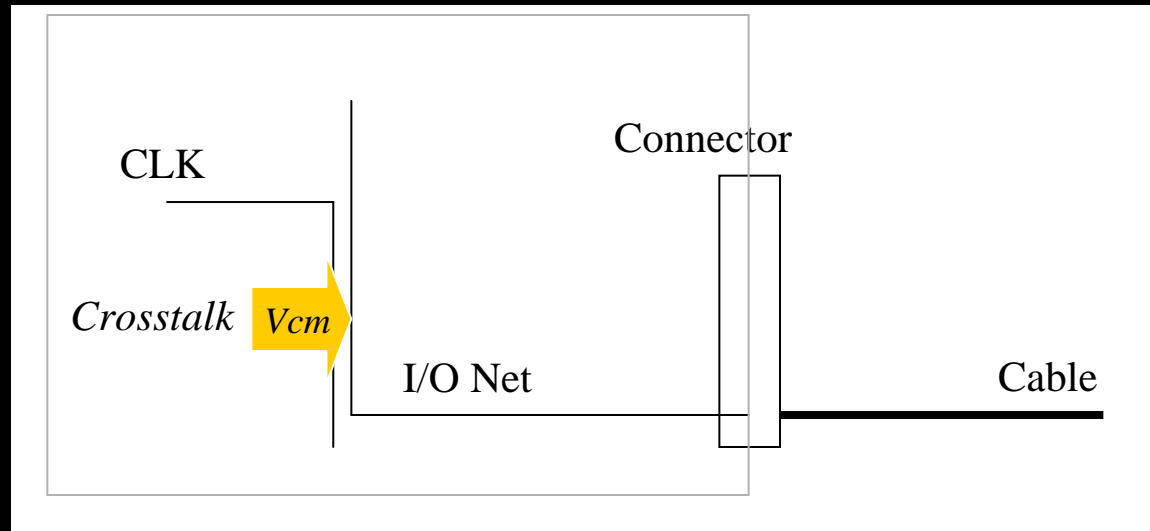


DRC #1: Clock trace w/ more than 2 vias



- v **Theory: Multiple changes in reference layers can cause excessive common mode current in the return path**

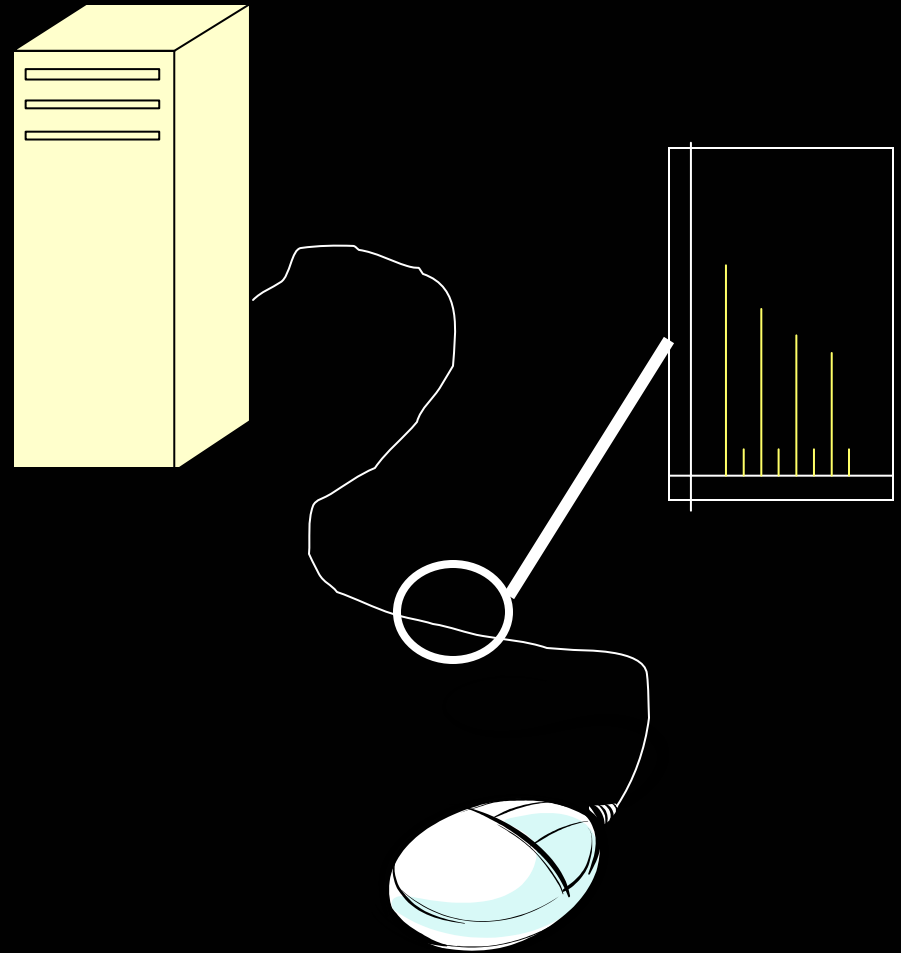
DRC Example #2: I/O Coupling



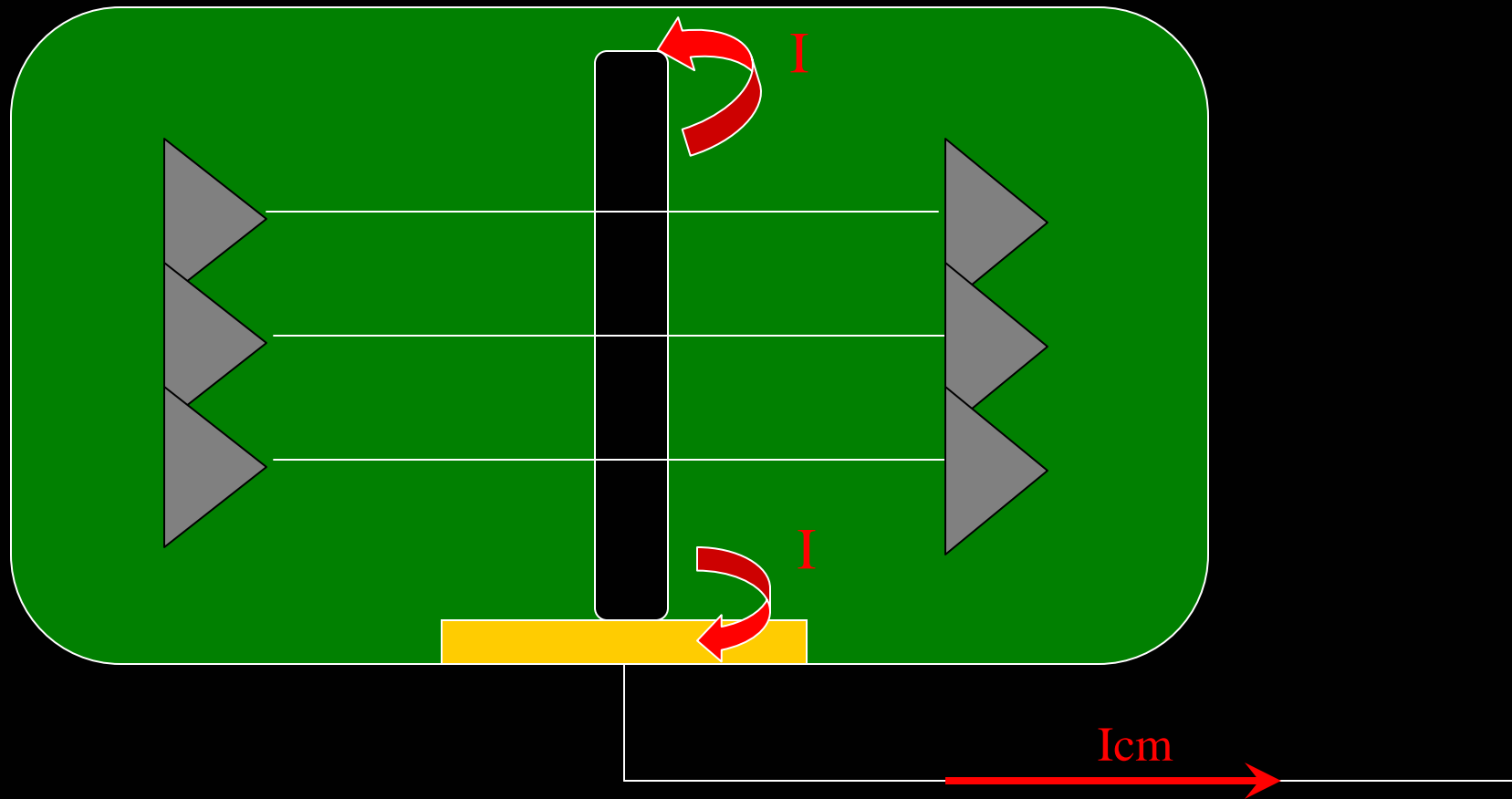
- v **Theory: I/O lines coupled to high speed nets receive noise, which is then taken off the board through cables. Cables have large loop areas, leading to increased EMI.**

I/O Coupling Example

- ✓ **Ideally: Current Flows back and forth in the wire**
- ✓ **Attaching a current probe shows that is not the case.**
- ✓ **How does the outgoing current return?**
- ✓ **Any currents sneaking out through cable will radiate back.**
- ✓ **What is radiation proportional to?**



DRC #3: No Gap Crossing



How Many Rules?

- ✓ **These rules need to be implemented by a person.**
- ✓ **If there are too many rules, then a person cannot keep track of them.**
- ✓ **If there are too few rules, you are missing crucial tests.**
- ✓ **So you probably want something on the order of 15-30 rules (as opposed to 100-200).**



Quiet Expert Rule Coverage

Example of some QE coverage:

- ✓ **Ground Layout/Integrity**
 - Gap crossings, return path changes
- ✓ **Power Supply Layout**
 - Adequate trace widths
- ✓ **Signal Trace Layout**
 - Minimizing Loop Area, avoiding dangerous configurations
 - Crosstalk parallelism
- ✓ **Rules are also customizable!!**

General Rules for
designing PCBs

EMC Expertise

Corporate Wide Expertise

DRC Rules for checking designs

EMC Expertise

EMC Expertise

Quiet Expert

EMC Expertise

Quiet Expert

EMC Expertise

Quiet Expert

EMC Expertise

Quiet Expert

EMC Expertise

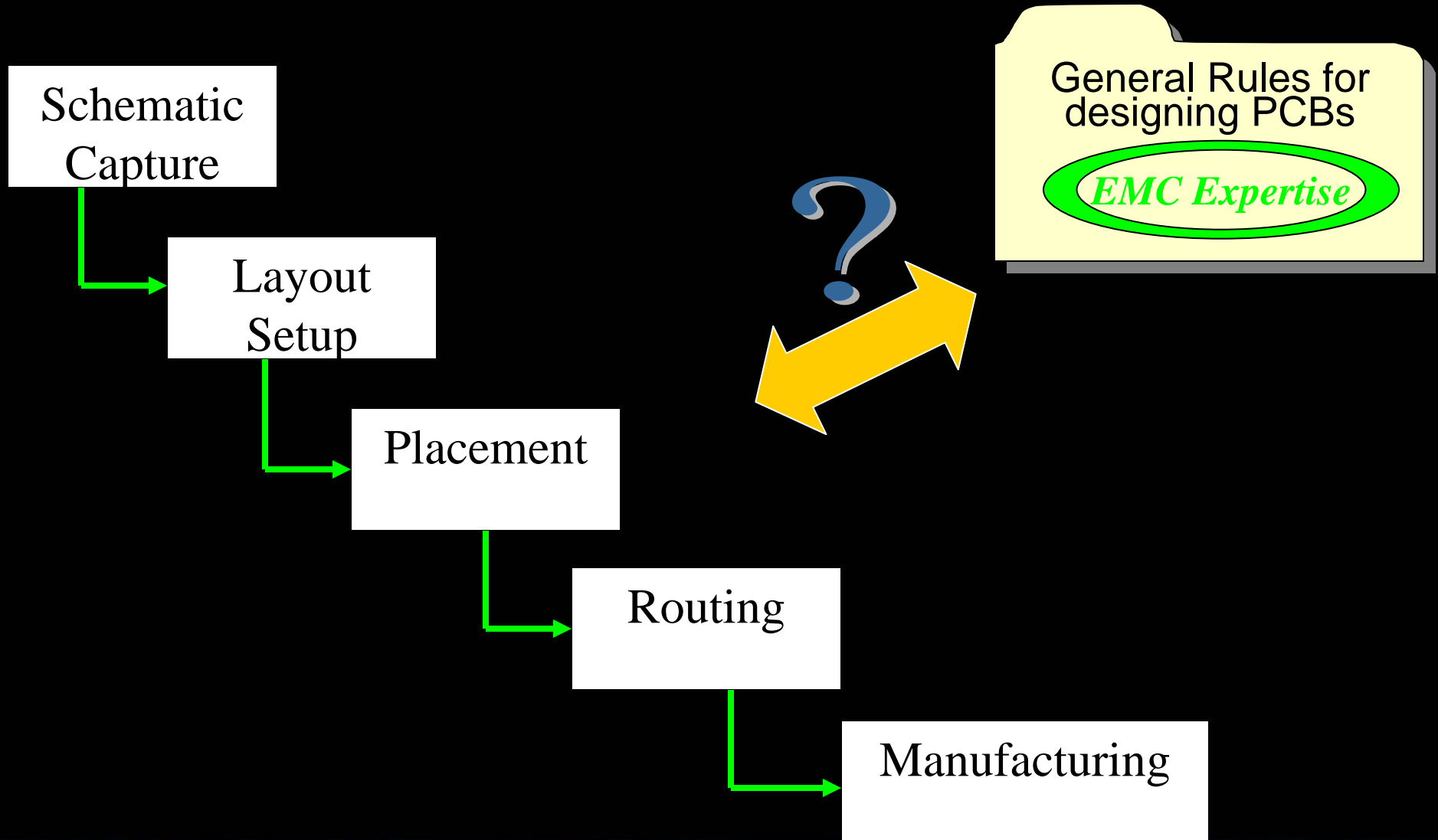
Quiet Expert

EMC Expertise



Corporate Wide Design Team usage

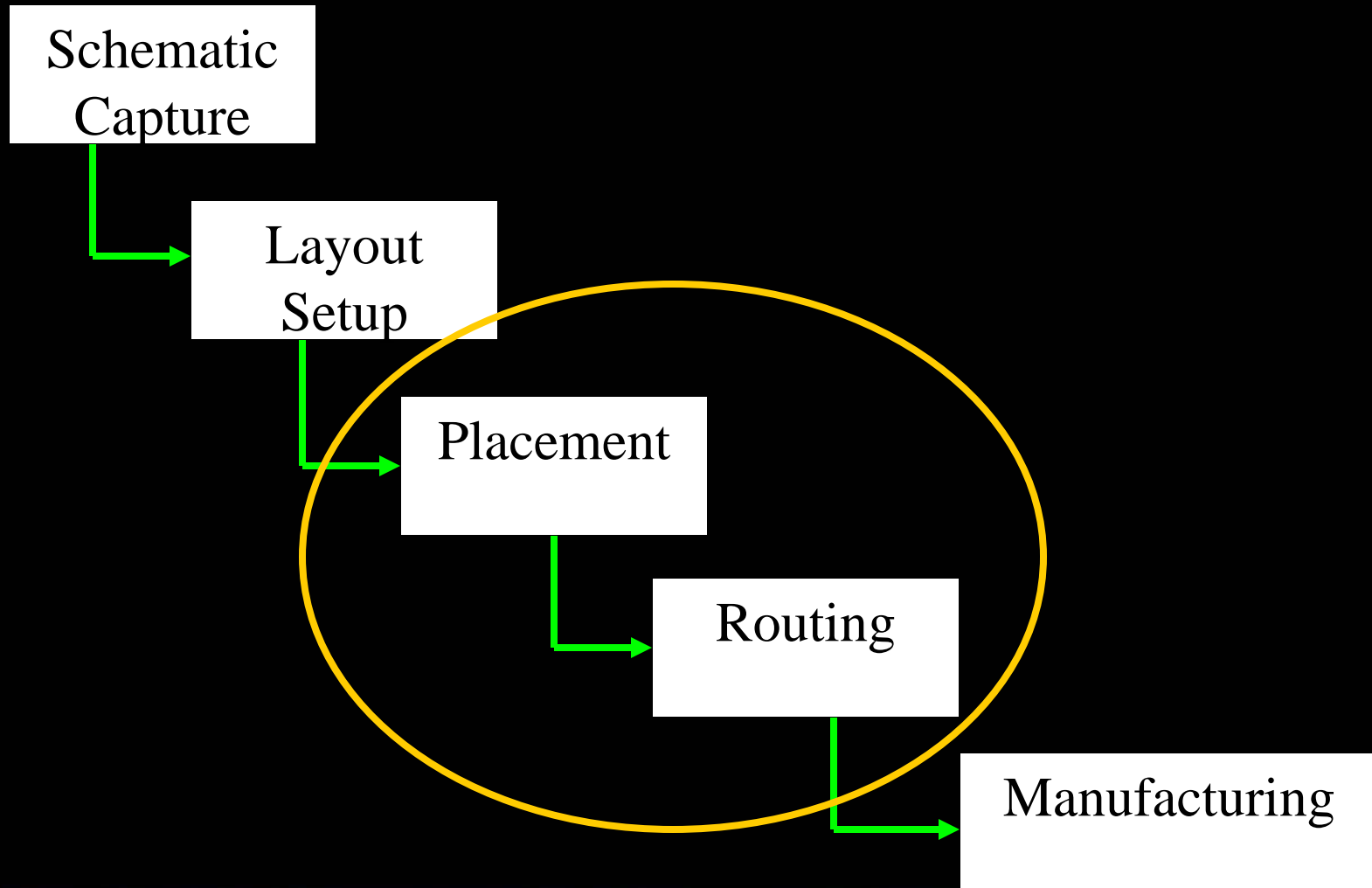
General Current Design Flow



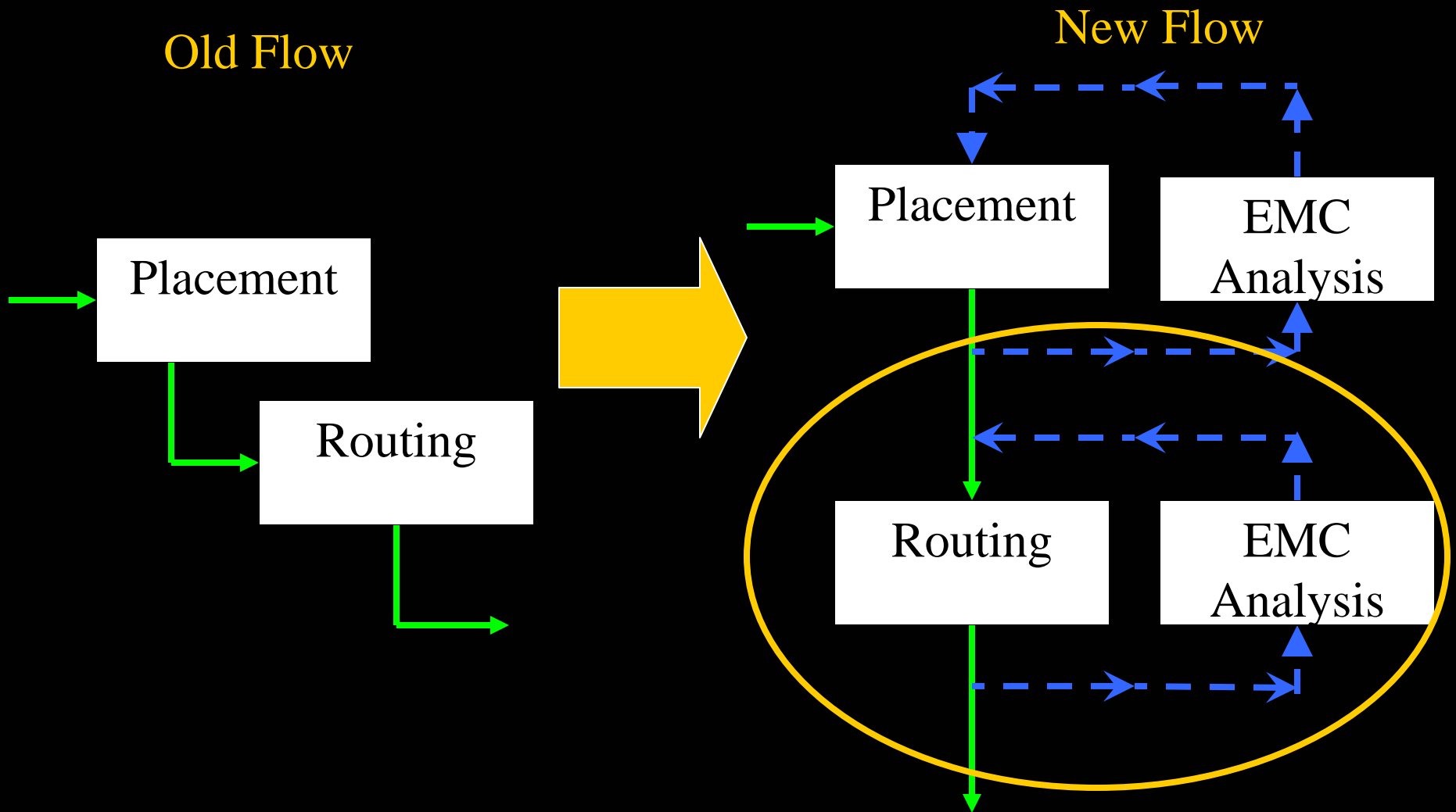
Chapter 5

How to Implement An EMI Methodology

Current Design Flow

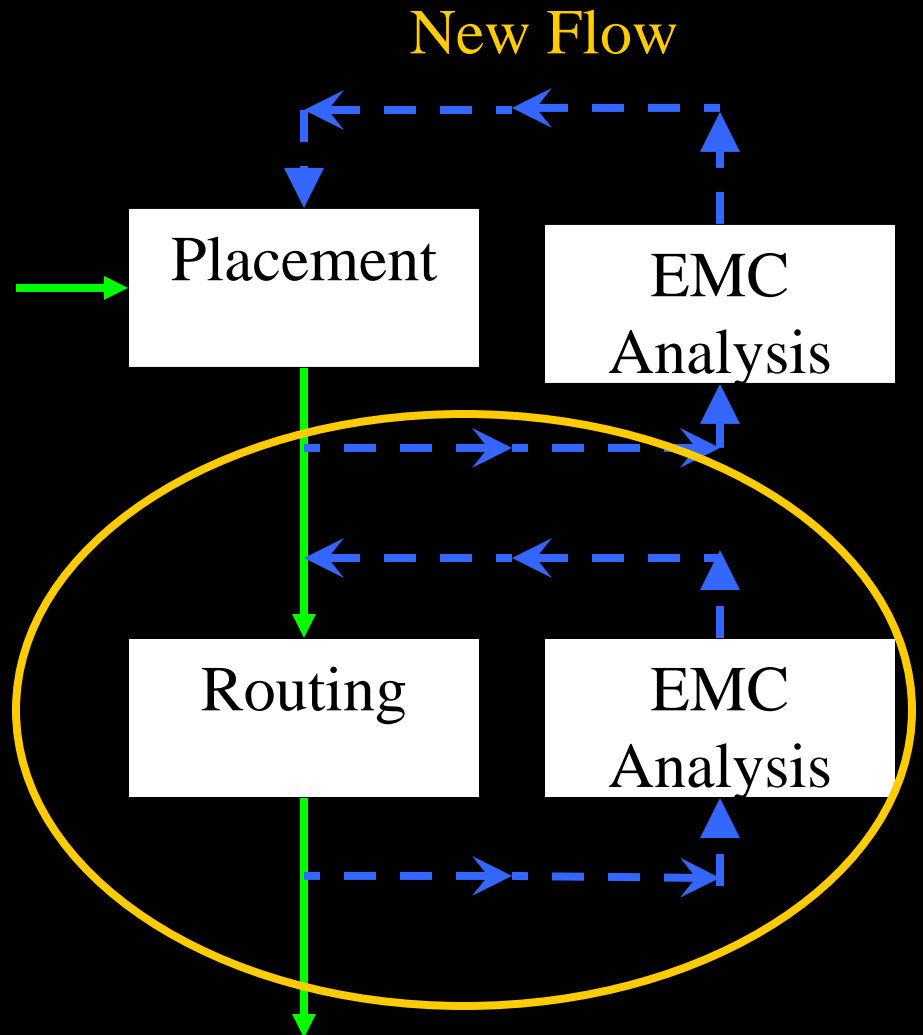


During Place and Route

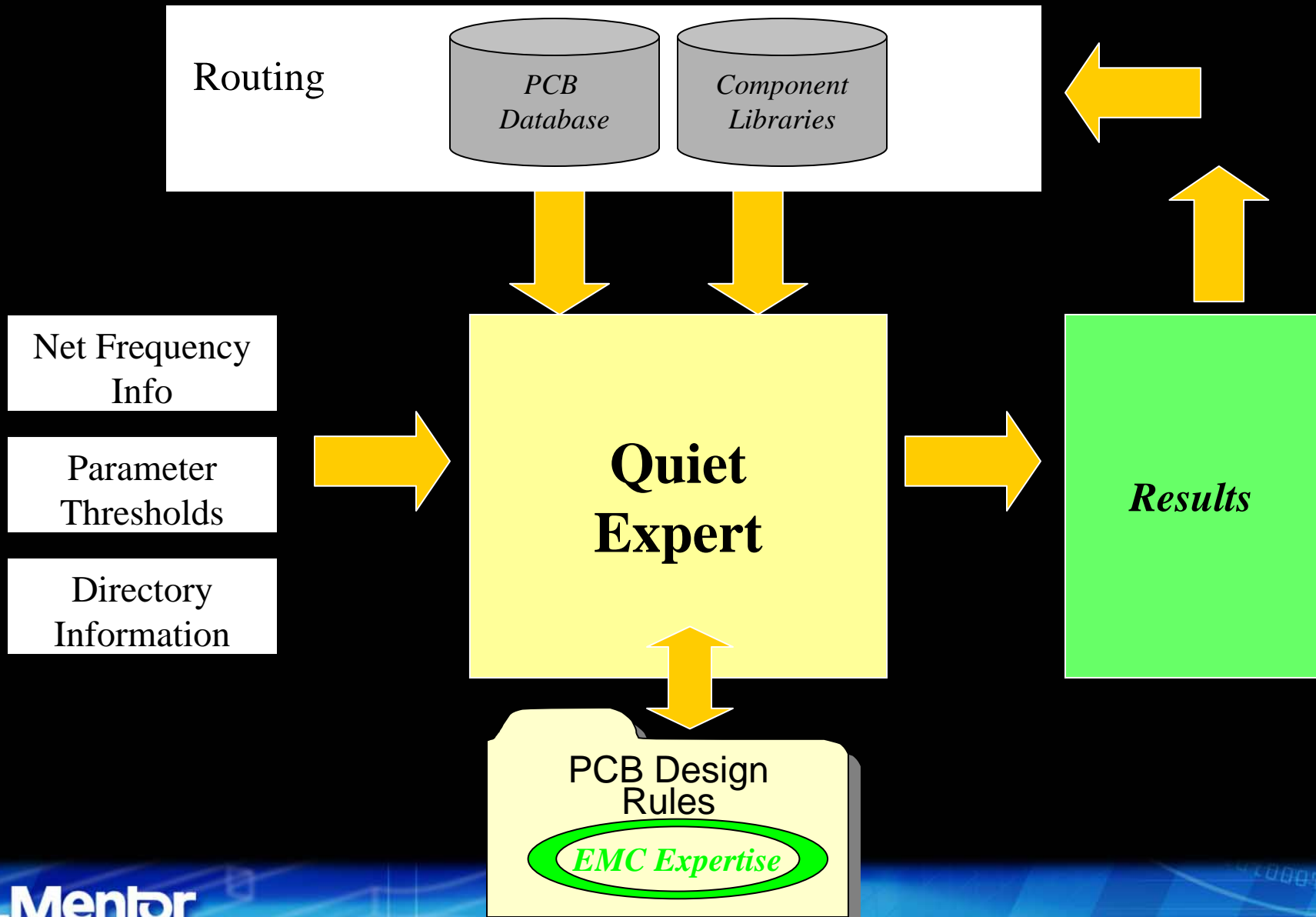


Requirements for New Analysis Loop

- ✓ **Fast**
- ✓ **Easy to Use**
- ✓ **Integrated**
- ✓ **Show you exactly where the problem exists**
 - Highlight net, pin, component or segment
 - Show items around the net causing the problem

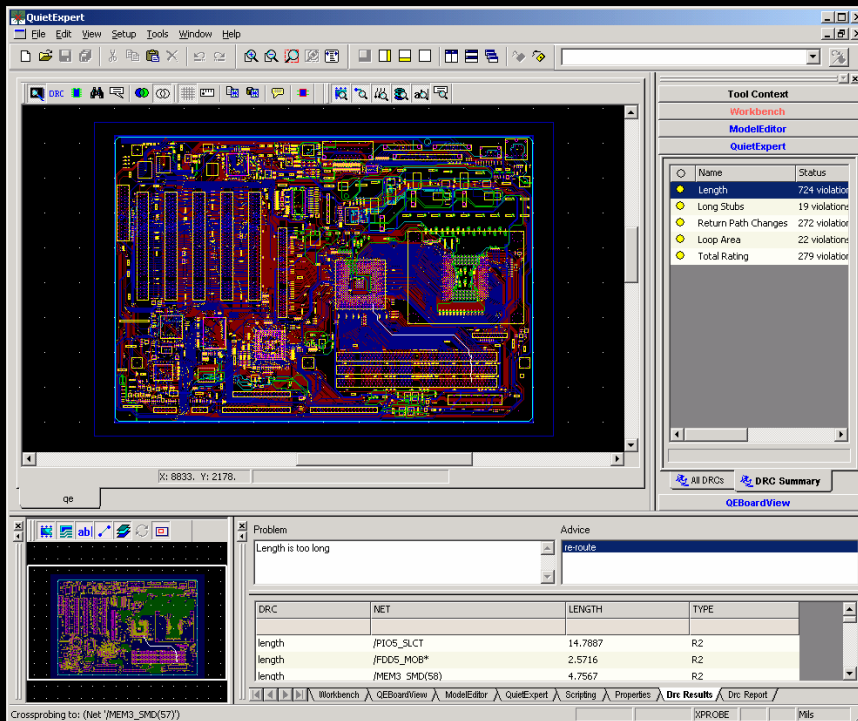


EMC Analysis Tool: Quiet Expert



QUIET Expert

“Two tools in one”



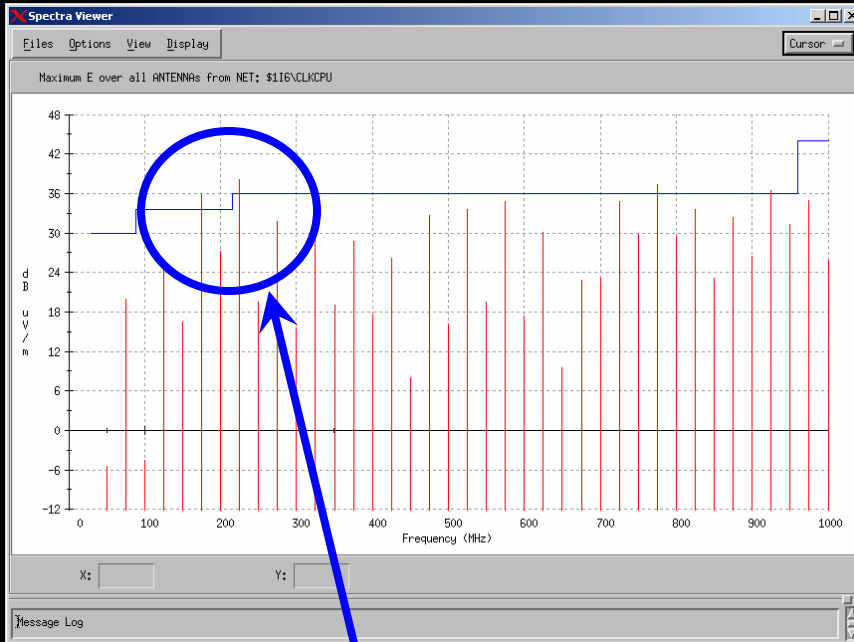
- **An EXPERT System**

- Solves EMI problem like a Engineer not a computer
- Makes intelligent assumptions for missing data

- **A PCB Rule Checker**

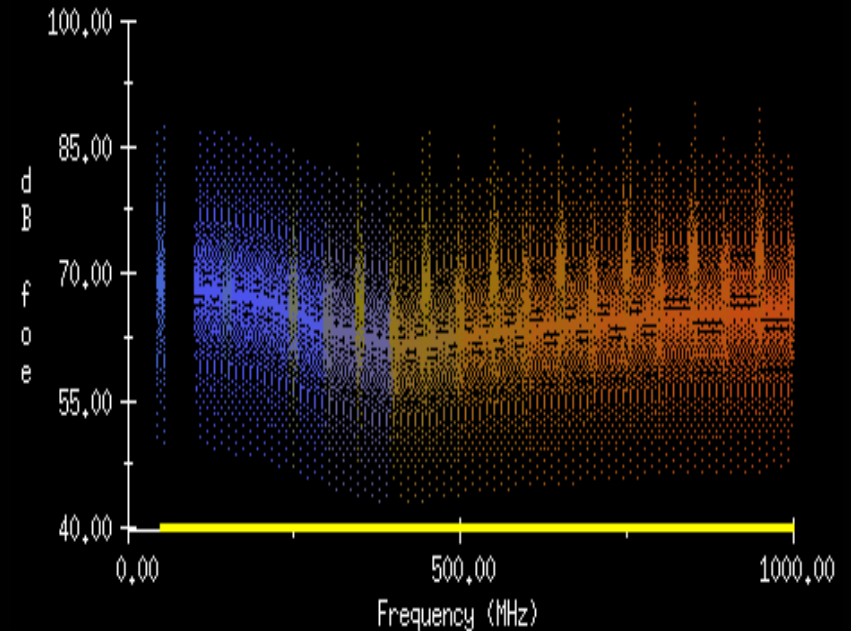
- Physical AND Electrical checks possible
- High-level language with access to ALL-level data.

What Results would be helpful?



“EMI Compliance is missed by 2dB-uV/m at 224MHz”

“The far field measurement is showing too much EMI above 800MHz”



DRCs make EMC simpler

- ✓ **Understandable**
- ✓ **Show you where the problem exists**
 - Highlight net, pin, component or segment
 - Show items around the net causing the problem
- ✓ **Describe why it is a problem**
- ✓ **Give advice on how to fix the problem**

Where?

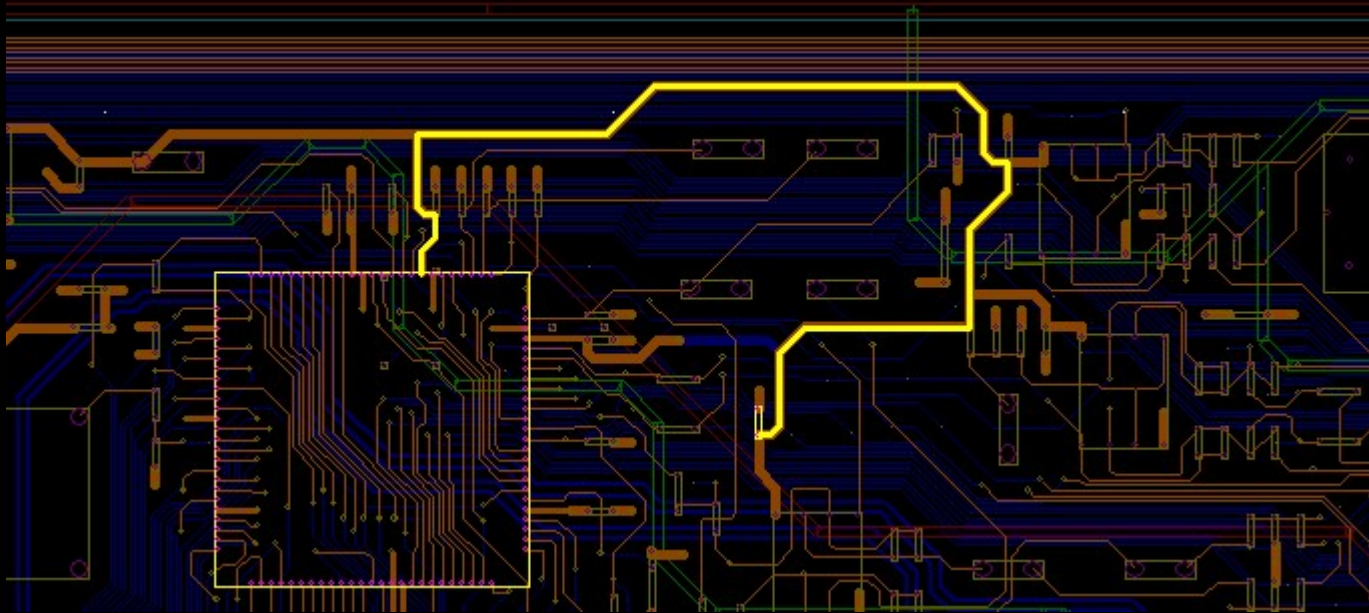
Why is it a problem?

How do I fix it?

Example of Good Rules

- v **Gap Crossing DRC**: Do not route critical high-speed nets over gaps in ground/power plane.
- v **Decoupling DRC**: Do not put the decoupling capacitor on a chip more than 5mm away from its power pin.

Decoupling CAP DRC



Problem: Pin to Decap Path length (12mm) more than maximum (5mm).

Advice: Reroute highlighted segment to reduce length

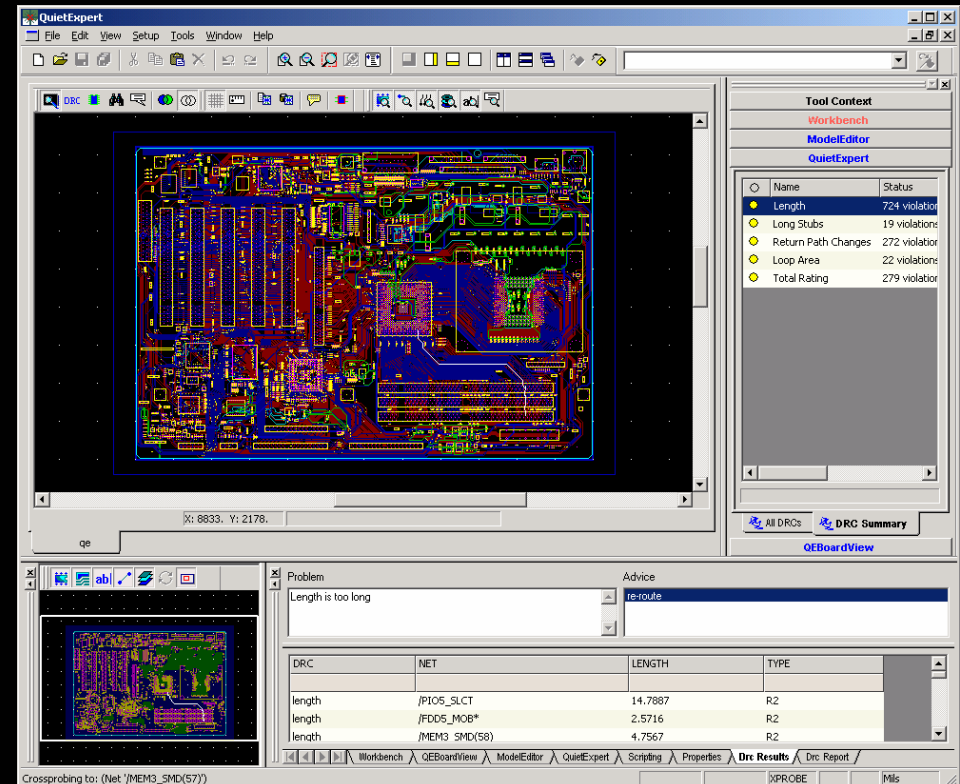
Decisions Process on Results

- ✓ **Designer must be involved in some capacity in making layout changes**
 - Mechanical considerations
 - Schedule considerations
 - Prioritization of rules
- ✓ **Communication of results is key, especially at the end of the layout cycle**
- ✓ **Trade-offs are usually necessary**

Quiet Expert Tool Features

Quiet Expert

- **Integrated Analysis Environment**
- **Quantitative information for the EMC expert**
- **Advice and Solutions for the non EMC expert**
- **Easy to use**
- **Incorporates IP from the University of Missouri – Rolla (UMR) EMC Consortium**
- **Support all major CAD flows**



Enhanced GUI

Fast, accurate board viewer

Flow Control

DRC List

World View window

Problems and advice

QuietExpert

File Edit View Setup Tools Window Help

Tool Center

- Workbench
- ModelEditor
- QuietExpert

Name	Status
Length	724 violations
Long Stubs	19 violations
Return Path Changes	22 violations
Loop Area	22 violations
Total Rating	279 violations

X: 8833, Y: 2178.

World View

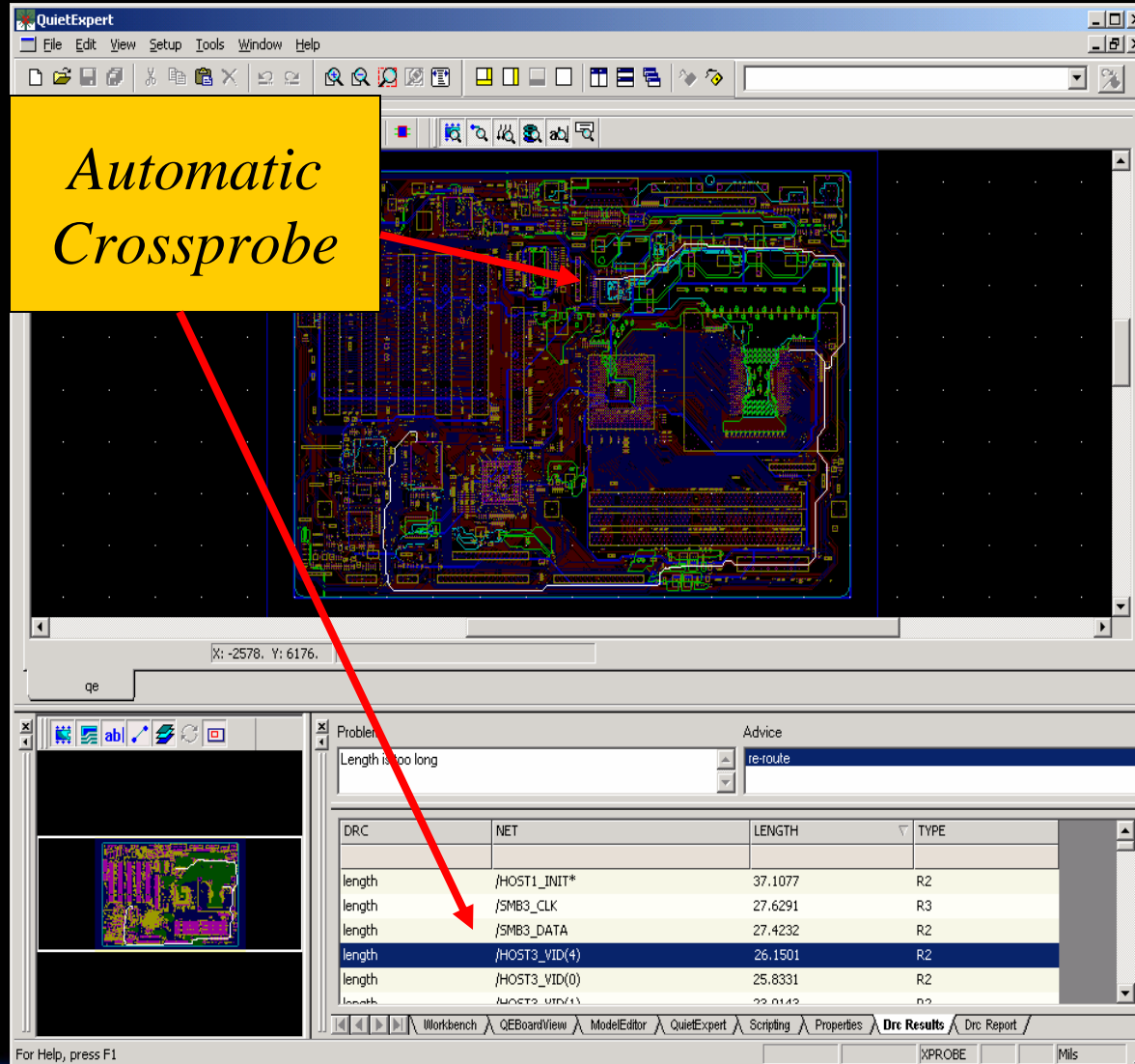
Problem: Length is too long

Advice: re-route

DRC	NET	LENGTH	TYPE
length	/PIOS_SLCT	14.7887	R2
length	/FDD5_MOB*	2.5716	R2
length	/MEM3_SMD(58)	4.7567	R2

Crossprobing to: (Net '/MEM3_SMD(57)')

DRC Results Cross Probe



- ✓ DRC result cross probe to board viewer
- ✓ Highlighting controlled by user. Highlight by:
 - Part
 - Net
 - Segment
 - Pin, etc.
- ✓ Programming Language: TCL/TK

DRC Reporting Environment

*Problem:
Why is it a
problem?*

*Advice:
How do I Fix
it?*

The screenshot shows a software window titled "Output Window" with two main sections: "Problem" and "Advice".

Problem: Too many changes in return path

Advice: look at change points and try to eliminate return path changes

Below these sections is a table with the following data:

DRC	NET	CHANGES	FRE
return path	/N\$87993	40	500.
return path	/HOST1_INIT*	20	500.
return path	/SMB3_CLK	21	500.
return path	/SMB3_DATA	19	500.
return path	/PIO5_SLIN*	32	500.

The interface also includes a navigation bar at the bottom with buttons for Workbench, QEBoard/View, ModelEditor, QuietExpert, Scripting, Properties, Drc Results, and Drc Report.

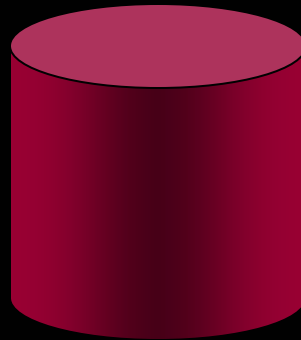
EMC Enterprise Collaboration



Layout Team



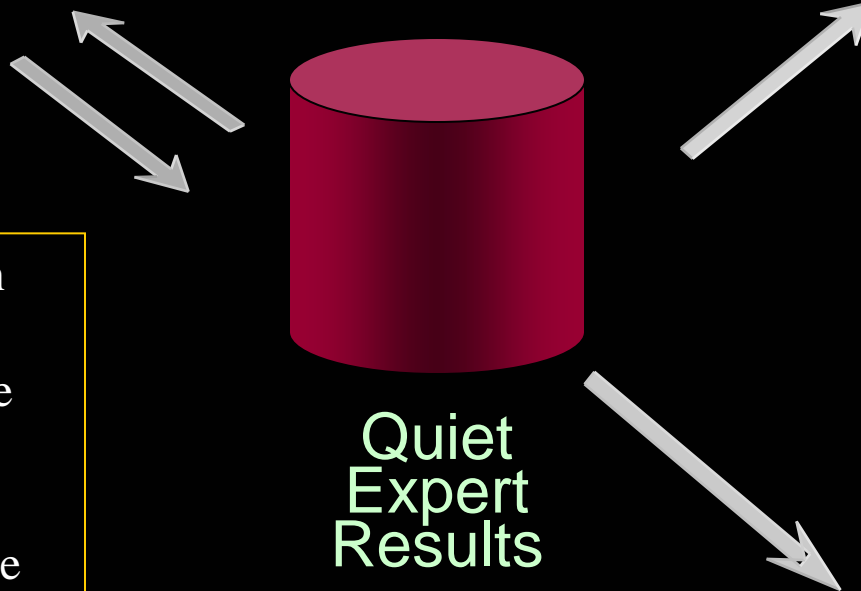
Design Team



Quiet Expert Results



EMC Team



Design Collaboration ties the design team together, allowing the same information to flow through the different groups in the design flow.

Enhanced Modeling Editor

The screenshot displays the 'Part Model Editor' window. On the left, there are input fields for Name (875947470), D/A (Digital), Family (CMOS), Cpd (0 pF), Dt (0 ns), Iocd (0 mA/MHz), Pkg (875947470), and Heat Sink. The main area contains a table with columns: Signal, Pin, Type, Analog, ClkPin, ClkDiv, SupplyPin, V(A), and V(D). A dropdown menu is open over the 'Type' column, listing options: BiDir, Driver, Receiver, BiDir, Voltage, and Null. The 'Driver Pin Model Editor' dialog box is open, showing fields for Name (VHC_OUT_tc7sh86u), Type (Driver), Analog/Digital (Analog selected), Oscillator (unchecked), Freq Min/Max (0 MHz), Rise/Fall (1.2 nsec), Vmin/Vmax (0, 3.3), Isc (57.5 mA), and Capacitance (0 pF). Buttons for OK, Cancel, Apply, Clear, and Reset are visible.

Signal	Pin	Type	Analog	ClkPin	ClkDiv	SupplyPin	V(A)	V(D)
	Y20	BiDir	No					
	Y19	Driver	No					
	Y18	Receiver	No					
	Y17	BiDir	No					
	Y16	Voltage	No					
	Y15	Null	No					
	Y14	BiDir	No					
		Receiver	No					

*Pulldown
menus*

*Driver
Definitions*

**IBIS Model
import**

Summary

- ✓ **Proper layout of PCBs significantly reduces system EMI**
- ✓ **Early preparation in the design cycle is the best place to fix potential EMI problems**
- ✓ **EMI problems non-compliance, susceptibility, system pollution and self-pollution**
- ✓ **Minimizing I_{dm} and Loop Area(A) reduces both Differential and Common Mode radiation**
- ✓ **DRCs give the quickest, most cost effective, and most understandable method to solving EMI problems**

The background is a vibrant blue with a complex pattern of white and light blue lines, resembling a circuit board or data flow. The lines form various shapes, including rectangles, circles, and zig-zags, creating a sense of depth and technology. The overall aesthetic is clean and modern, typical of a corporate logo for a technology company.

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