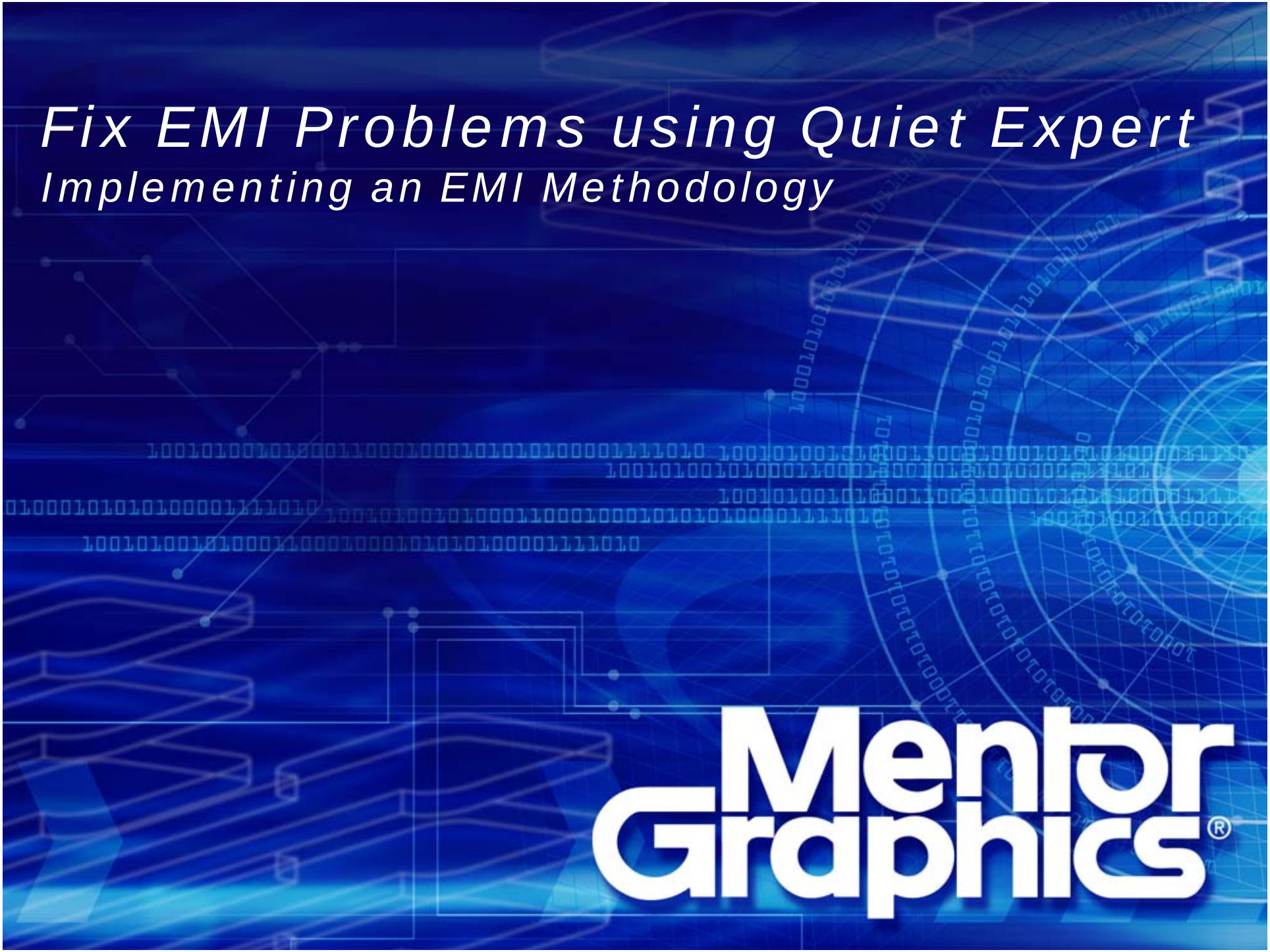
Fix EMI Problems using Quiet Expert

Implementing an EMI Methodology



Agenda

1. Today's EMI Problem
2. EMI Analysis Options
3. Causes of EMI
4. Design Rule Checks: Definition and Effectiveness
5. Implementing an EMC Methodology
6. Quiet Expert Tool Features

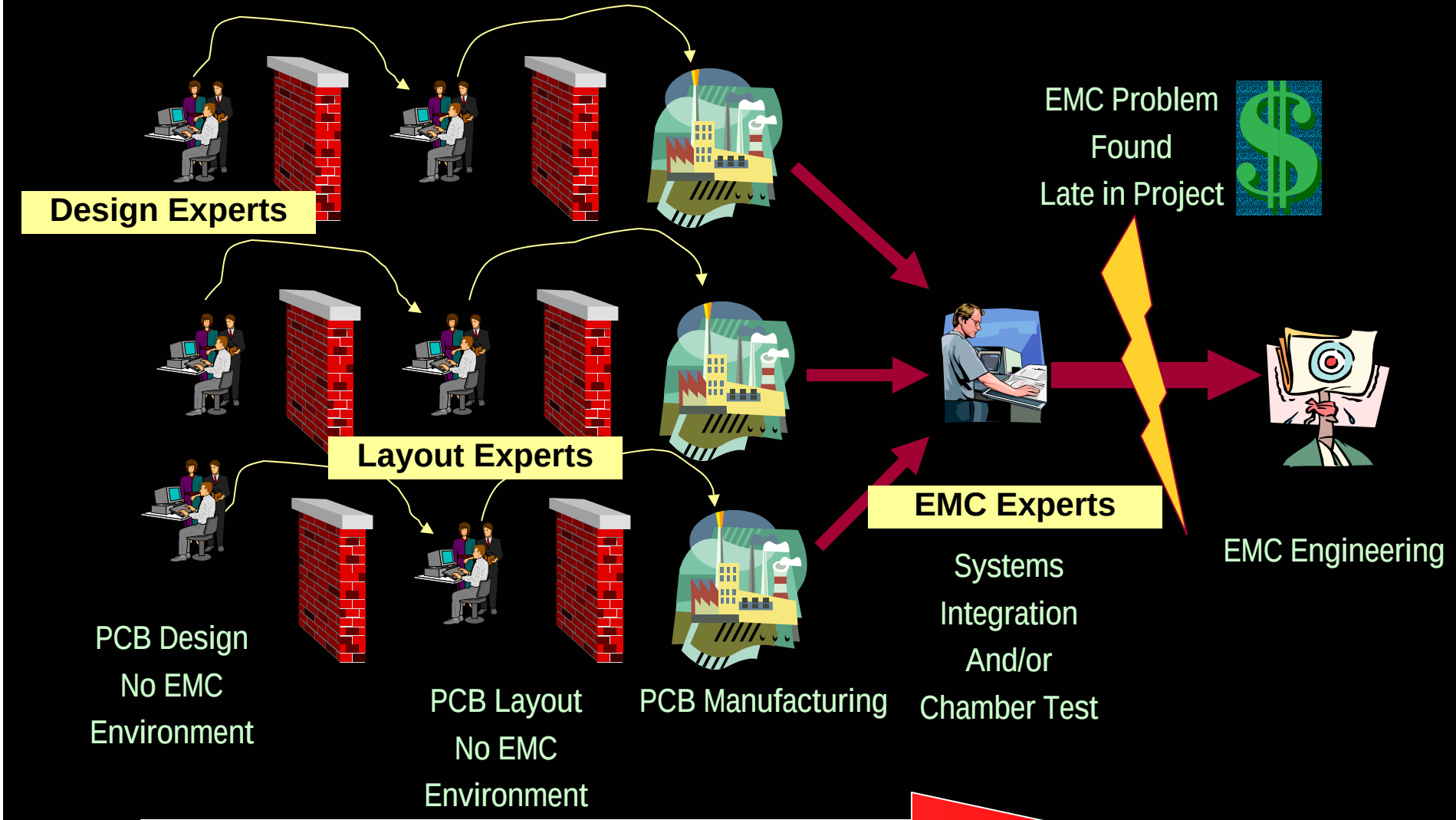
Goals for Today's Session

- **Provide non-EMC experts an understanding what causes EMC problems**
- **Why you DON'T need to know:**
  - **FDTD analysis**
  - **Far field vs. Near field**
  - **Horizontal Em measurements**
- **Understand good PCB layout practices with regards to EMC *and* signal integrity**
- **How to solve 75%-100% of your PCB EMC problems with a simple change in design flow.**
- **Understand good Design Rule Checks for EMC**

Chapter 1

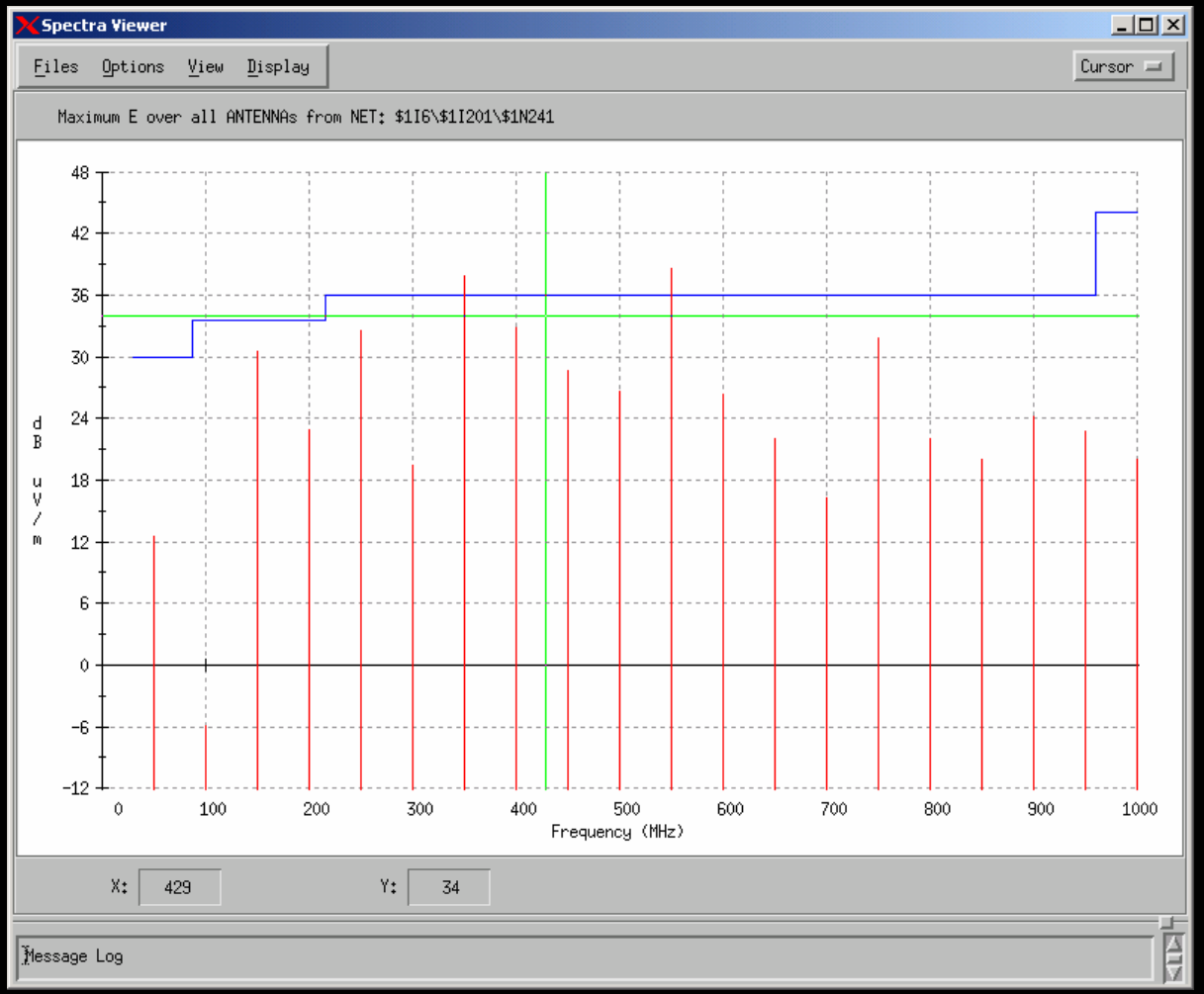
Today's EMI Problem

Customer Design Model

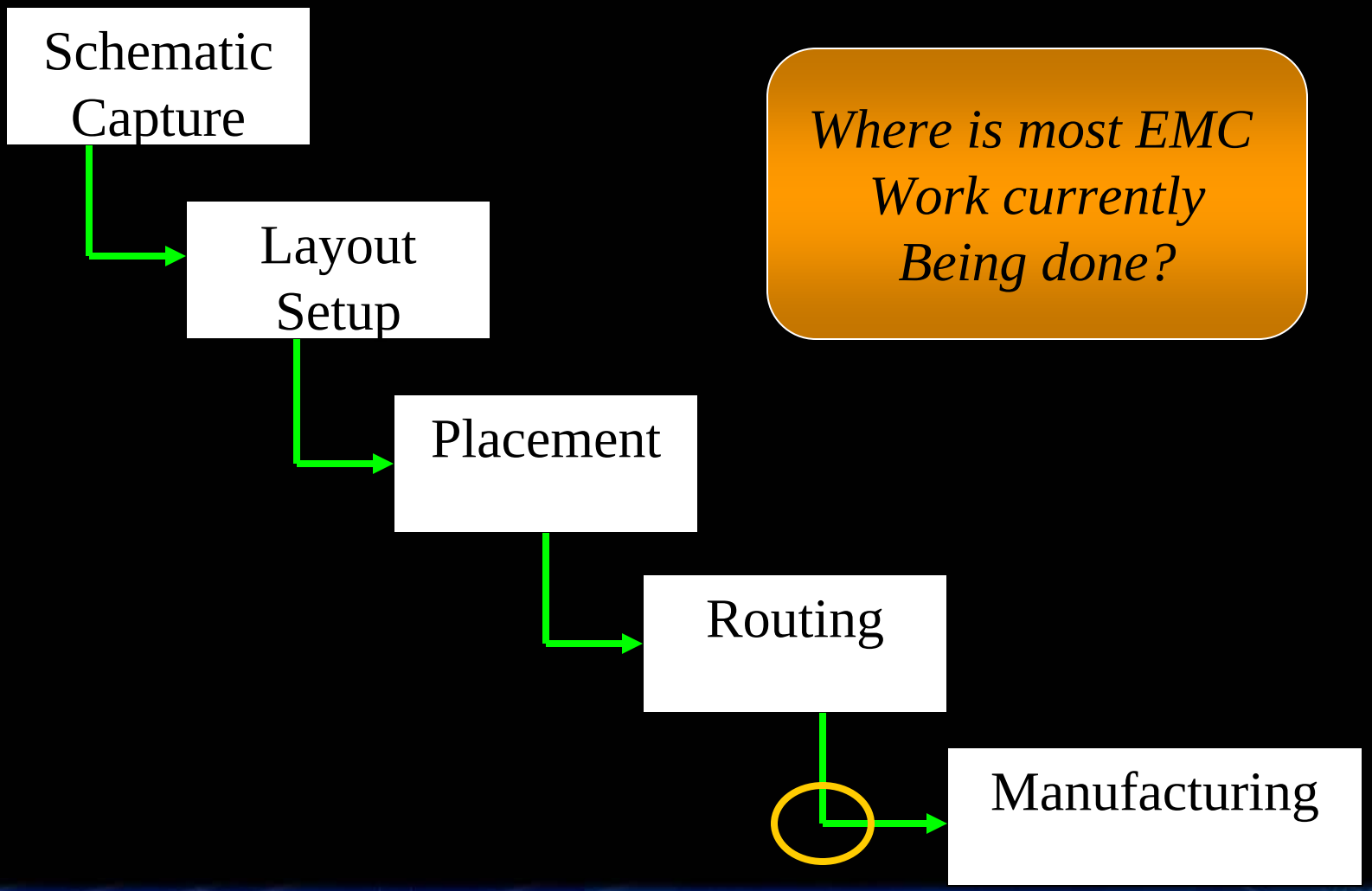


What does the EMC Expert see?

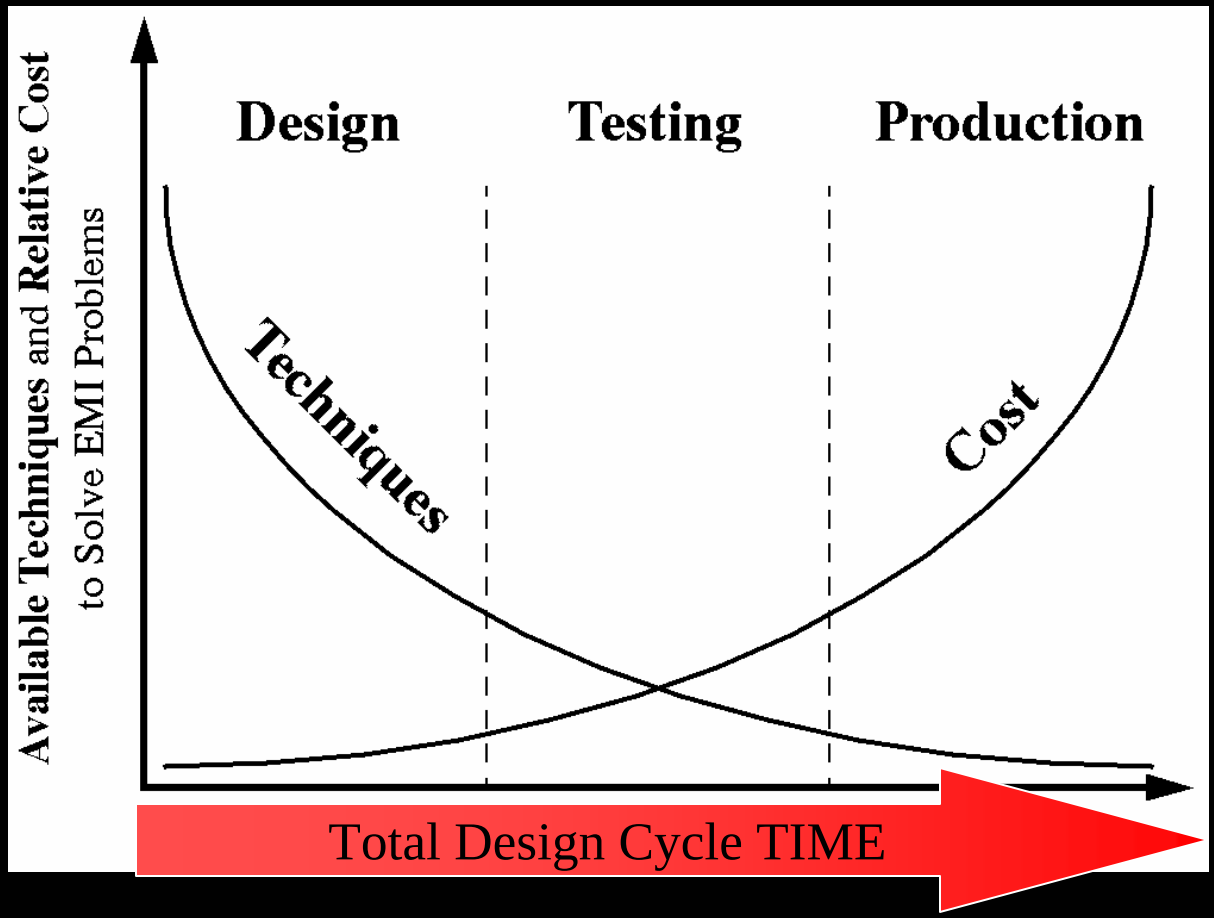
- Does this pass FCC regulations?
- What is the problem with this design?
- **Reduction of 2dB passes!**



General Customer Design Flow



When do I fix EMI problems?



Ref: Ott, H., Noise Reduction Techniques in Electronic Systems, 2nd ed., John Wiley & Sons, 1988, p. 6.

Chapter 2

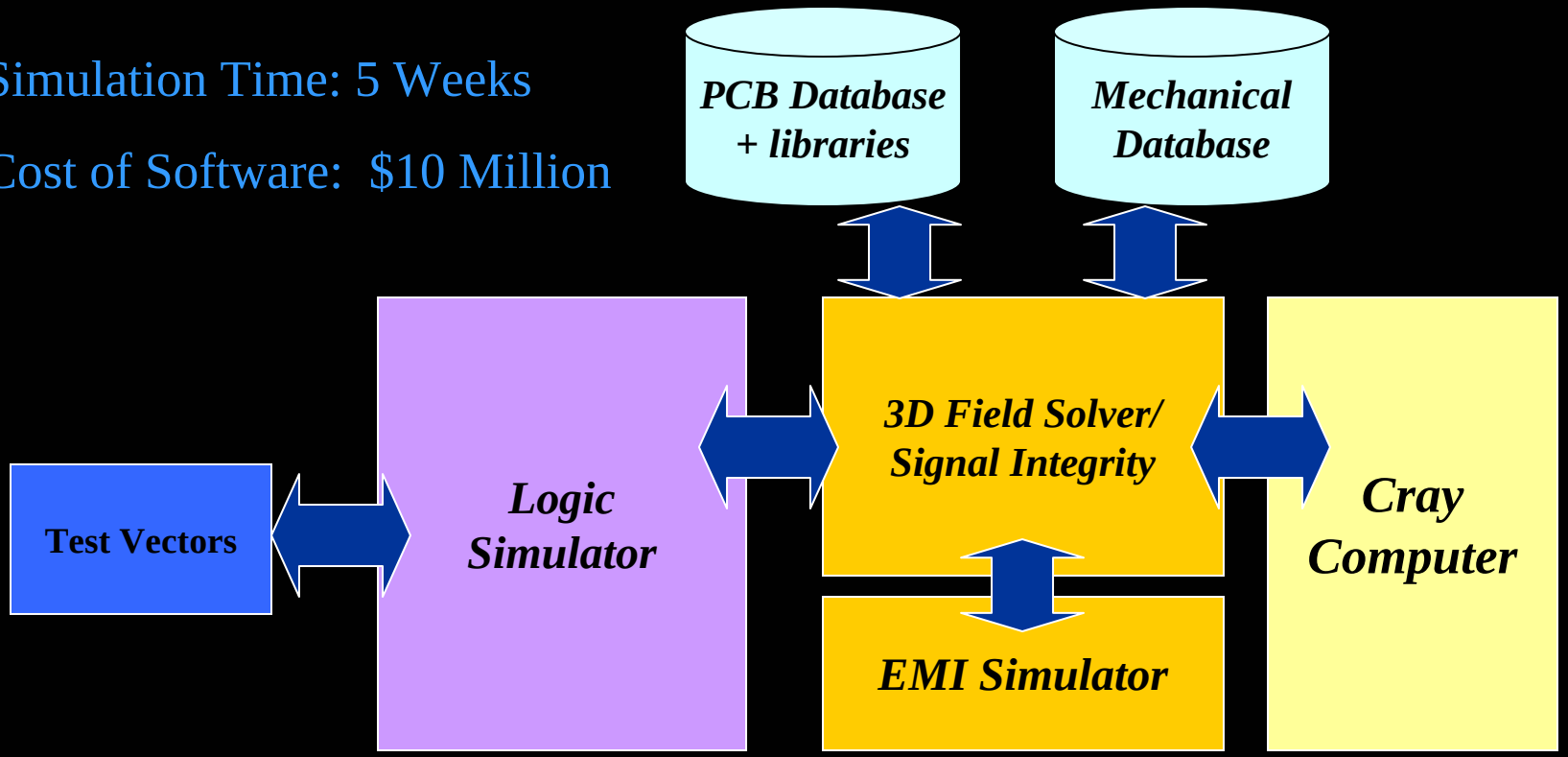
EMI Analysis Options

II. Analysis Options

- **Hope and Pray**
- **Simulation – Is it possible?**

Simulation Time: 5 Weeks

Cost of Software: $10 Million



What about Signal Integrity?

- Current SI simulation is considered to be good in the mV precision range.
- In EMI, uV noise on a good antenna can cause EMI Compliance failure
- Mechanisms that cause failure are not easy to identify or completely understood (much religious debate).
- Very small changes in input (e.g. duty cycle of a clock) can cause massive changes to measured EMI.

Other Analysis Options

- **Hand Check Design Rules**
  - **Works if you know your rules**
  - **Time Consuming**
  - **Prone to human error**
  - **Most companies have rules, but no automation or mechanism to implement and enforce them.**
- **Confidence in DRCs critical to effective methodology**

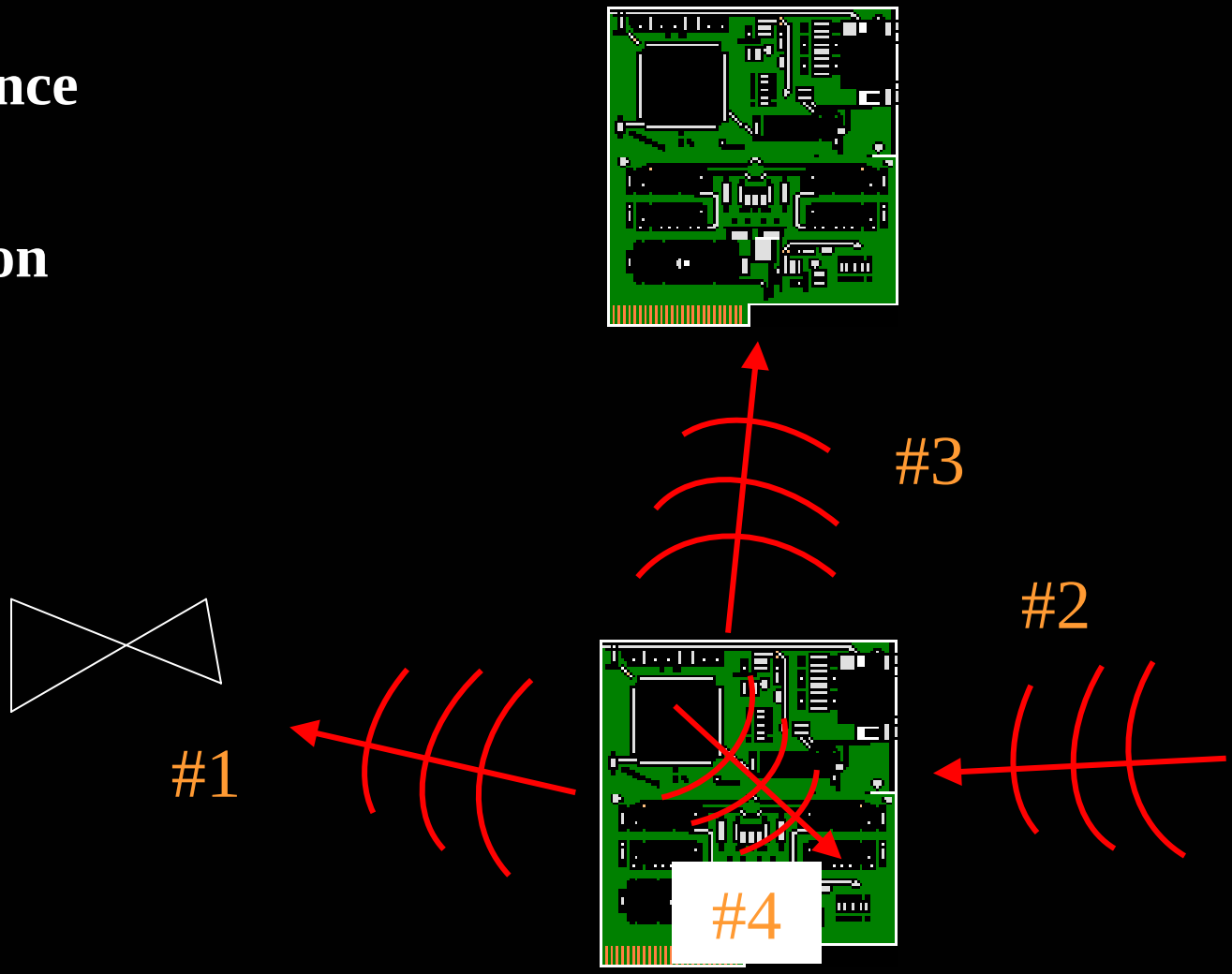
Chapter 3

Causes of EMC

Why the PCB should be your focus.

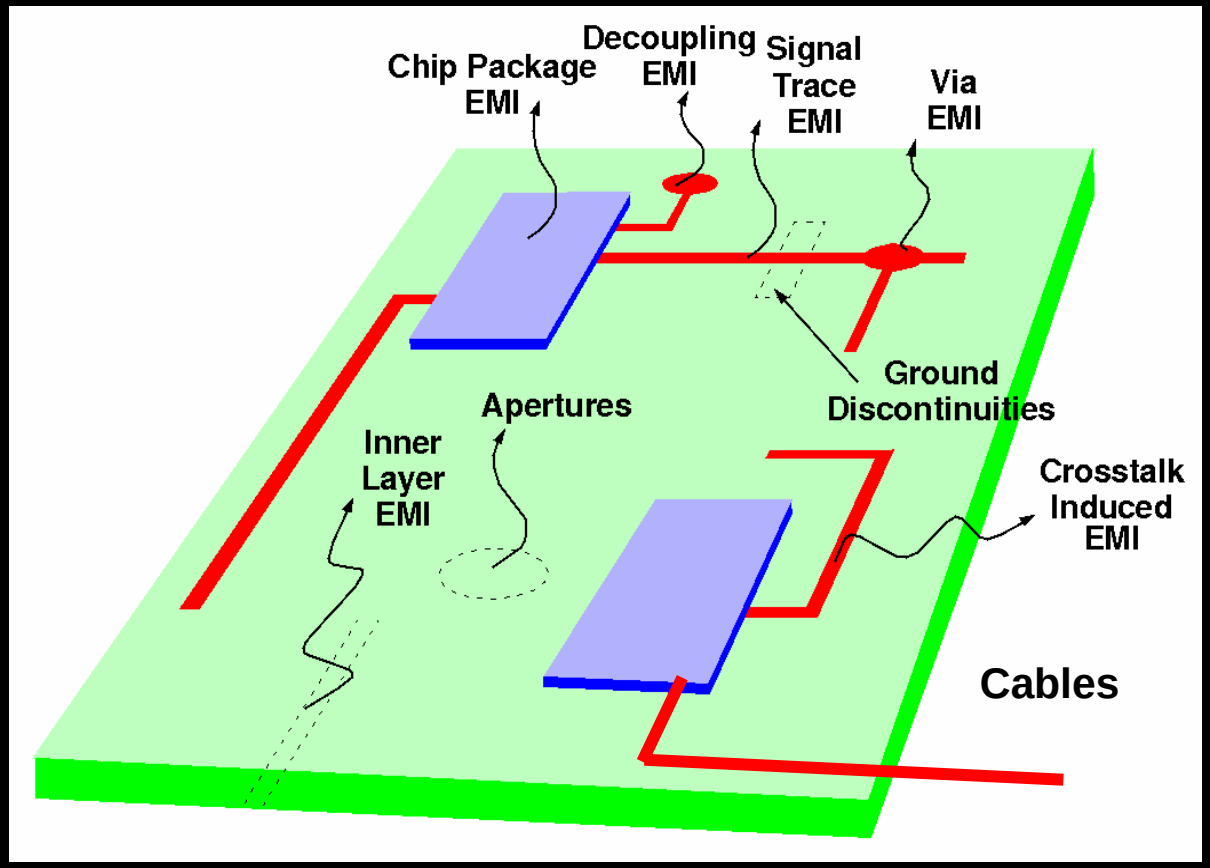
III. Top 4 Problems of EMC

1. **EMC Compliance**
2. **Susceptibility**
3. **System Pollution**
4. **Self Pollution**

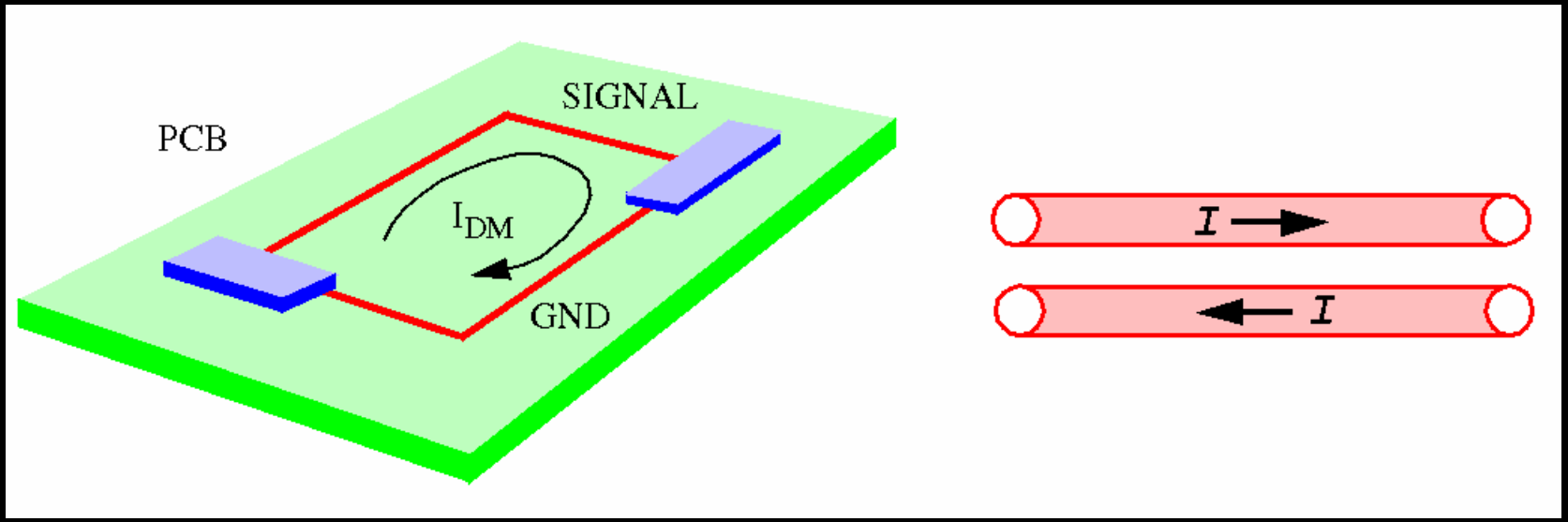


EMC Sources

- Chips
- Decoupling
- Signal Trace
- Via
- Ground plane
- Apertures
- Cables
- Crosstalk

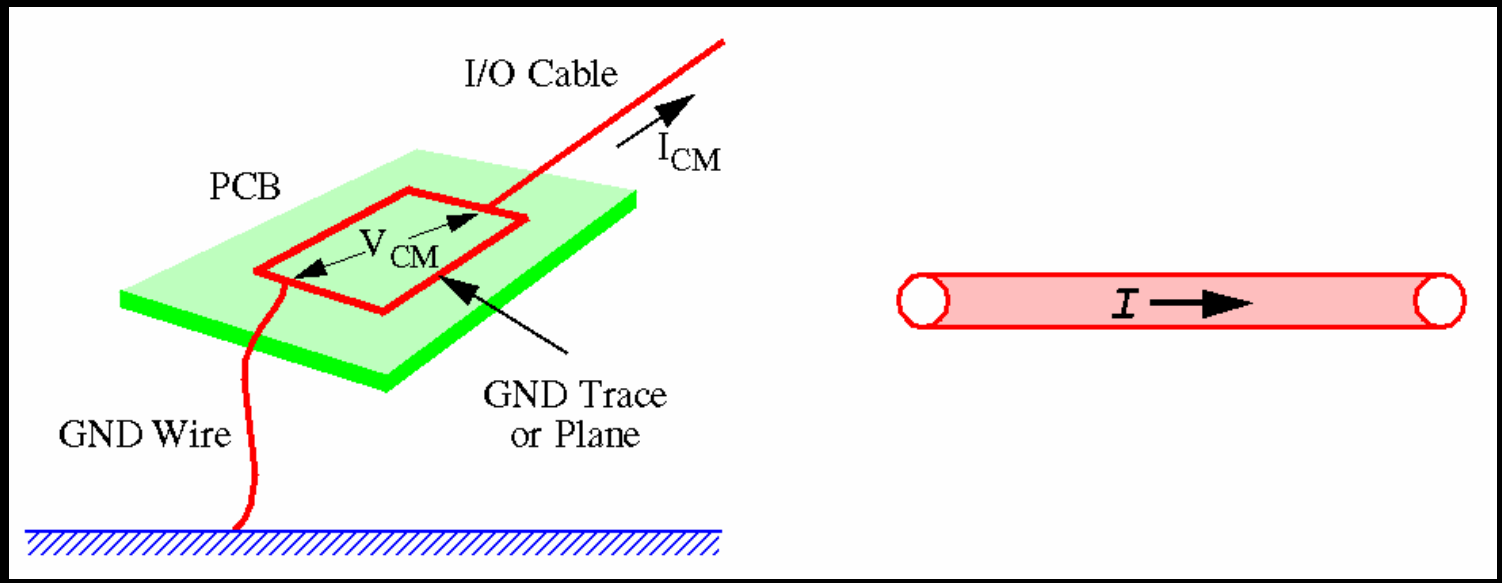


Differential Mode Radiation



- **Modeled as Loop Antenna**
- **Examples:**
  - **trace-trace, trace-plane, chip package, ground slot, ...**

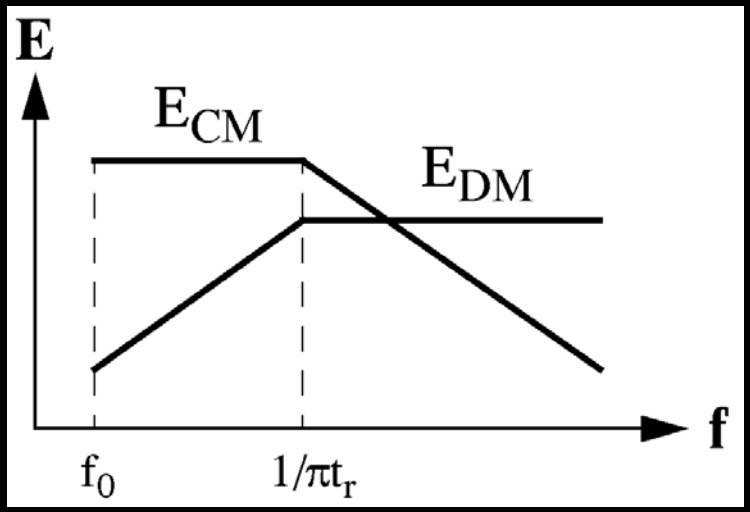
Common Mode Radiation



- **Modeled as Monopole Antenna**
- **Examples:**
  - **cable, cable shield, ...**

DM vs. CM Radiation

- **DM radiation:** $E_{DM} \propto \left(I_{DM} A\right) \frac{f^2}{r}$
- **CM radiation:** $E_{CM} \propto \left(I_{CM} L\right) \frac{f}{r} \propto \left(I_{CM} L \lambda\right) \frac{f^2}{r}$



DM and CM Control Techniques

- **DM emission control:**
  - minimize I_{DM} and A

$$E_{DM} \propto \left(I_{DM} A\right) \frac{f^2}{r}$$

- **CM emission control:**
  - minimize I_{DM} and A

$$E_{CM} \propto \left(I_{CM} L\right) \frac{f}{r} \propto \left(I_{CM} L \lambda\right) \frac{f^2}{r}$$

$$I_{CM} \propto \frac{V_{CM}}{Z_{CM}} \propto \frac{I_{DM} L_{CM}}{Z_{CM}} \propto \frac{I_{DM} A}{Z_{CM}}$$

- **Shielding is an effective but expensive solution for both DM and CM emission control**
  - e.g. stripline, enclosure, cable shield.

Minimizing I_{DM} and A

- Use logic families that are no faster than necessary.
- Use the lowest clock frequency possible.
- Use the longest risetime possible for all pulse signals

I_{DM}

- Keep all clock lines as short as possible.
- Tightly control the loop area of all high speed signals.
- Do not allow any traces to cross any gaps in the return plane.
- Provide a closely located return path for all critical signals.
- Provide at least one decoupling capacitor for each power pin.
- Use Design Rule Checks (DRCs) to minimize area

A

Chapter 4

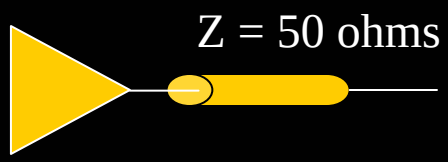
Design Rule Checks
Definition and effectiveness

Definitions

- **Design Rule Check (DRC): A ordinance or regulation that should be followed to insure proper operation of the design according to its specification.**
- **Examples:**

Signal Integrity

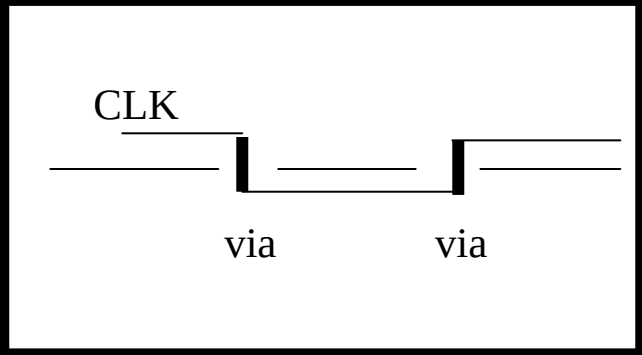
Match Impedance with Driver



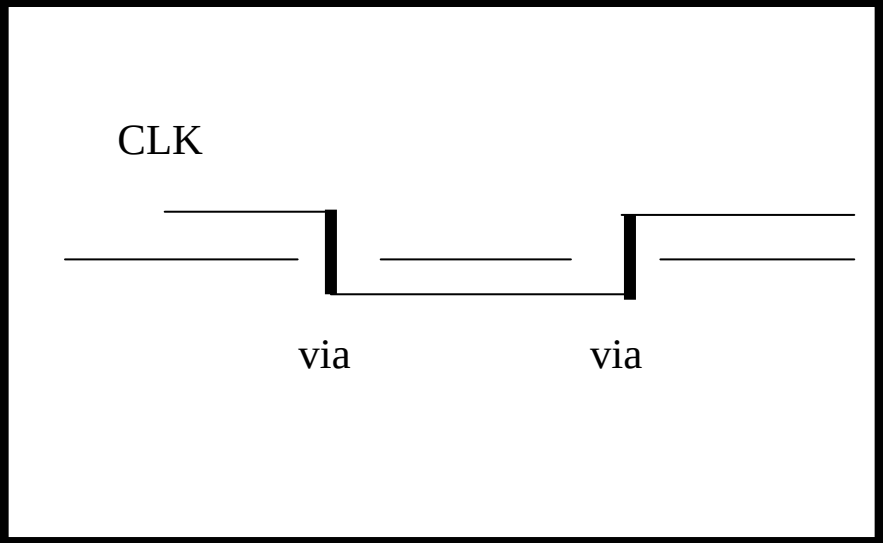
Zout = 50 ohms

EMC

No more than 2 vias (layer changes) on a clock trace

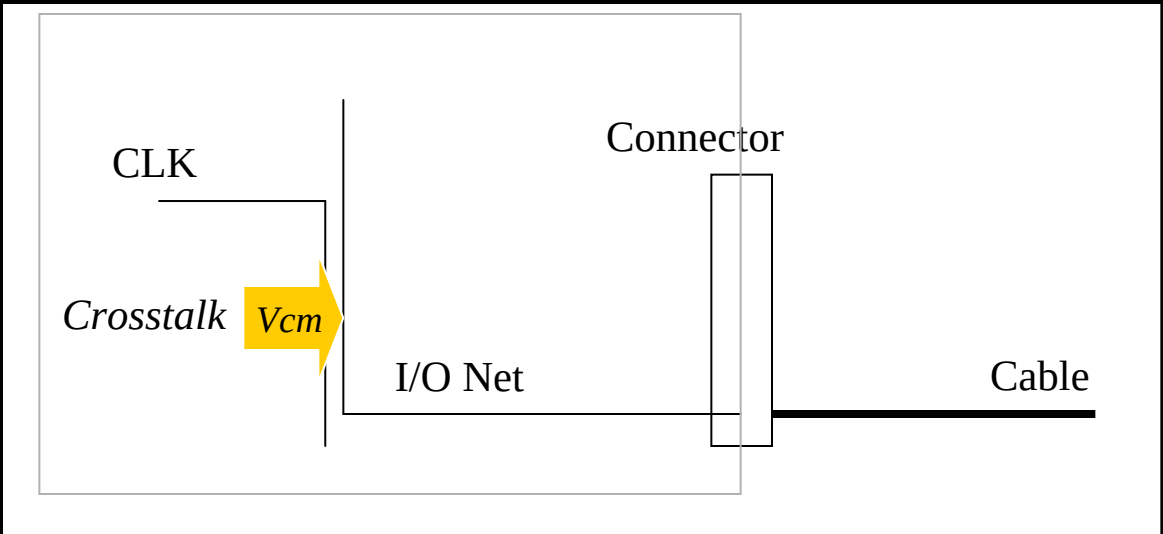


DRC #1: Clock trace w/ more than 2 vias



- **Theory: Multiple changes in reference layers can cause excessive common mode current in the return path**

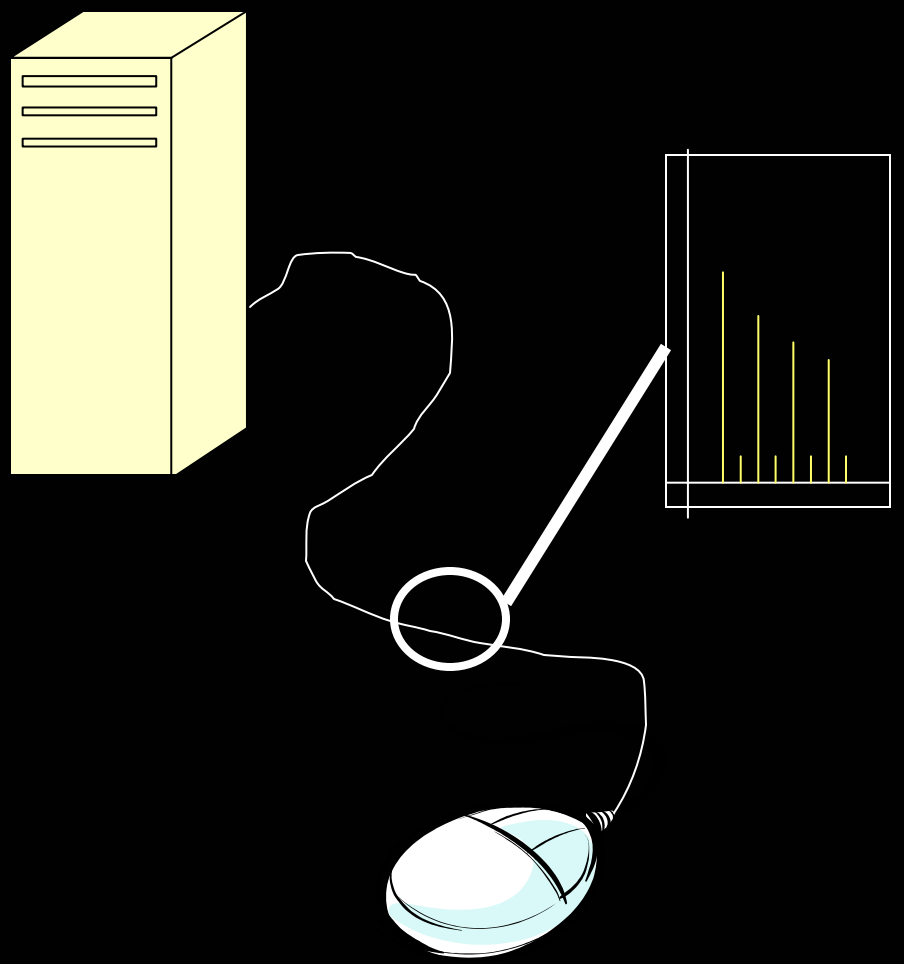
DRC Example #2: I/O Coupling



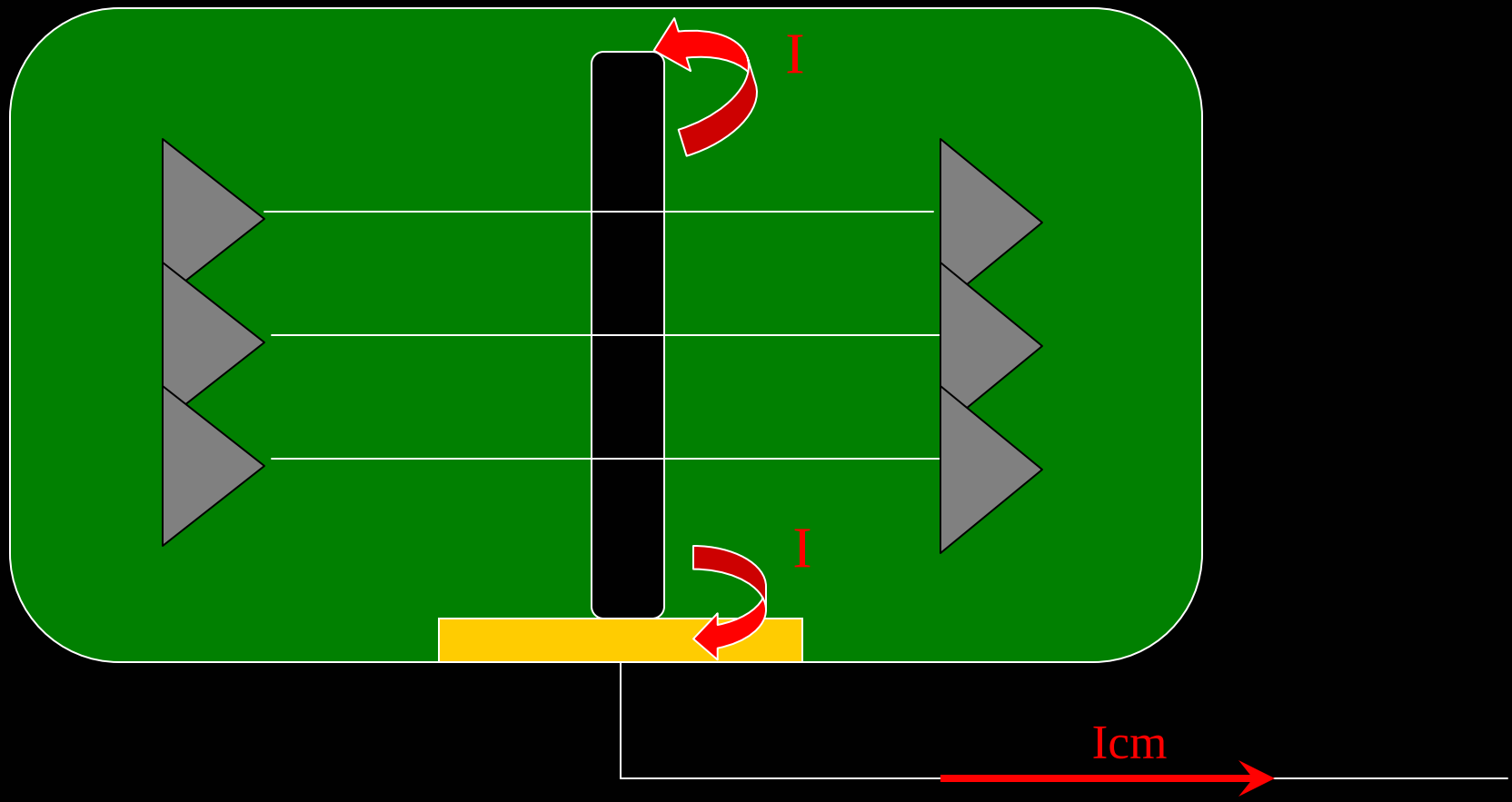
- **Theory: I/O lines coupled to high speed nets receive noise, which is then taken off the board through cables. Cables have large loop areas, leading to increased EMI.**

I/O Coupling Example

- Ideally: Current Flows back and forth in the wire
- Attaching a current probe shows that is not the case.
- How does the outgoing current return?
- Any currents sneaking out through cable will radiate back.
- What is radiation proportional to?



DRC #3: No Gap Crossing



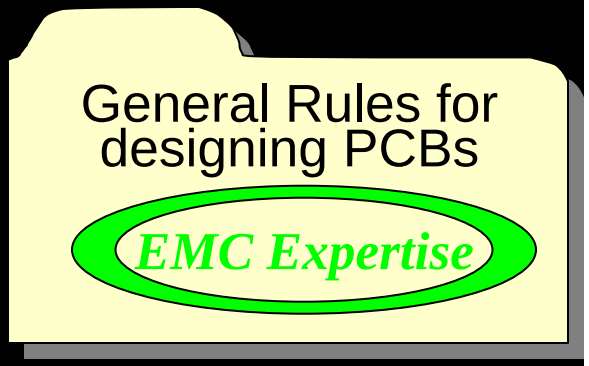
How Many Rules?

- These rules need to be implemented by a person.
- If there are too many rules, then a person cannot keep track of them.
- If there are too few rules, you are missing crucial tests.
- So you probably want something on the order of 15-30 rules (as opposed to 100-200).

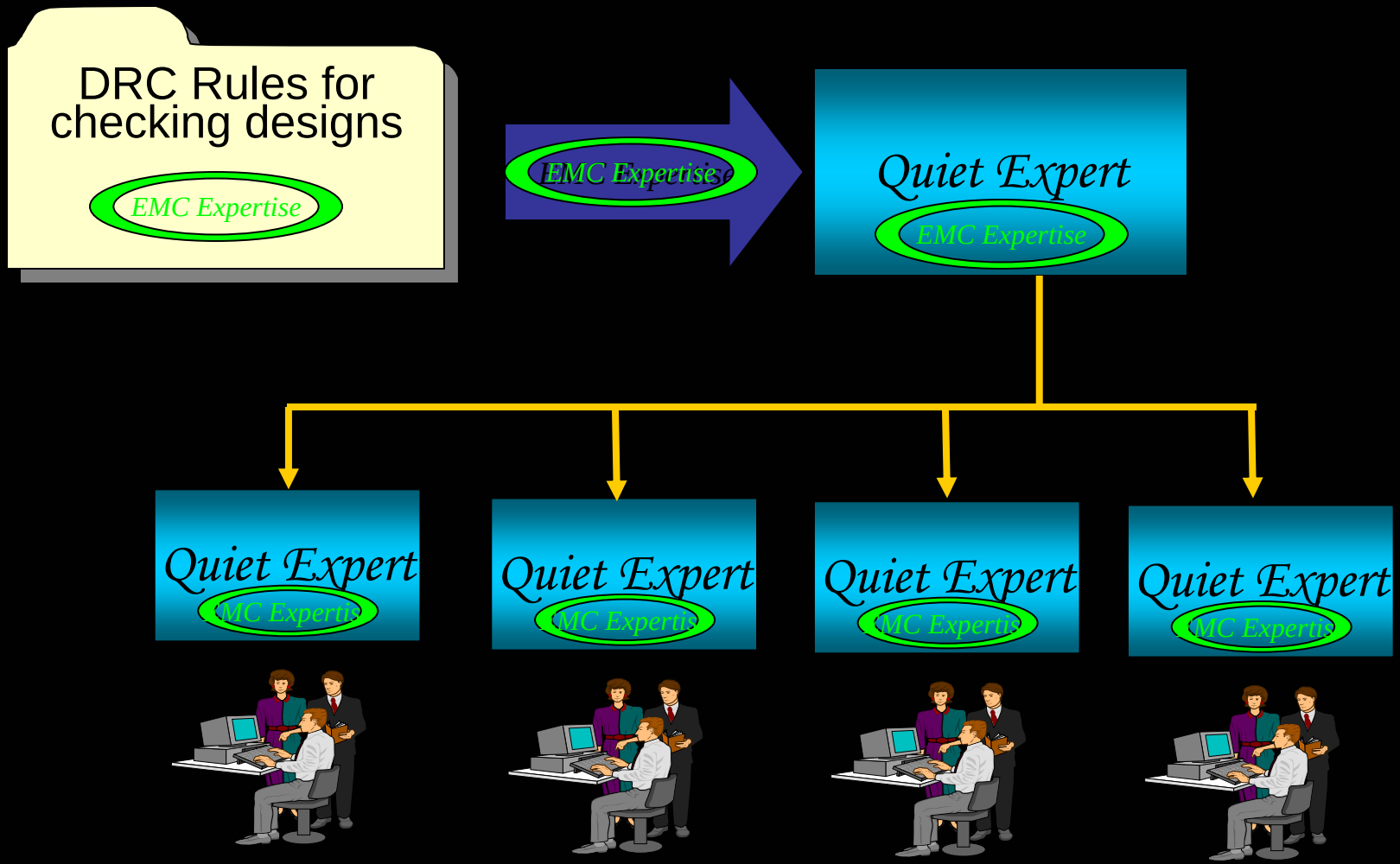
Quiet Expert Rule Coverage

Example of some QE coverage:

- **Ground Layout/Integrity**
  - **Gap crossings, return path changes**
- **Power Supply Layout**
  - **Adequate trace widths**
- **Signal Trace Layout**
  - **Minimizing Loop Area, avoiding dangerous configurations**
  - **Crosstalk parallelism**
- **Rules are also customizable!!**

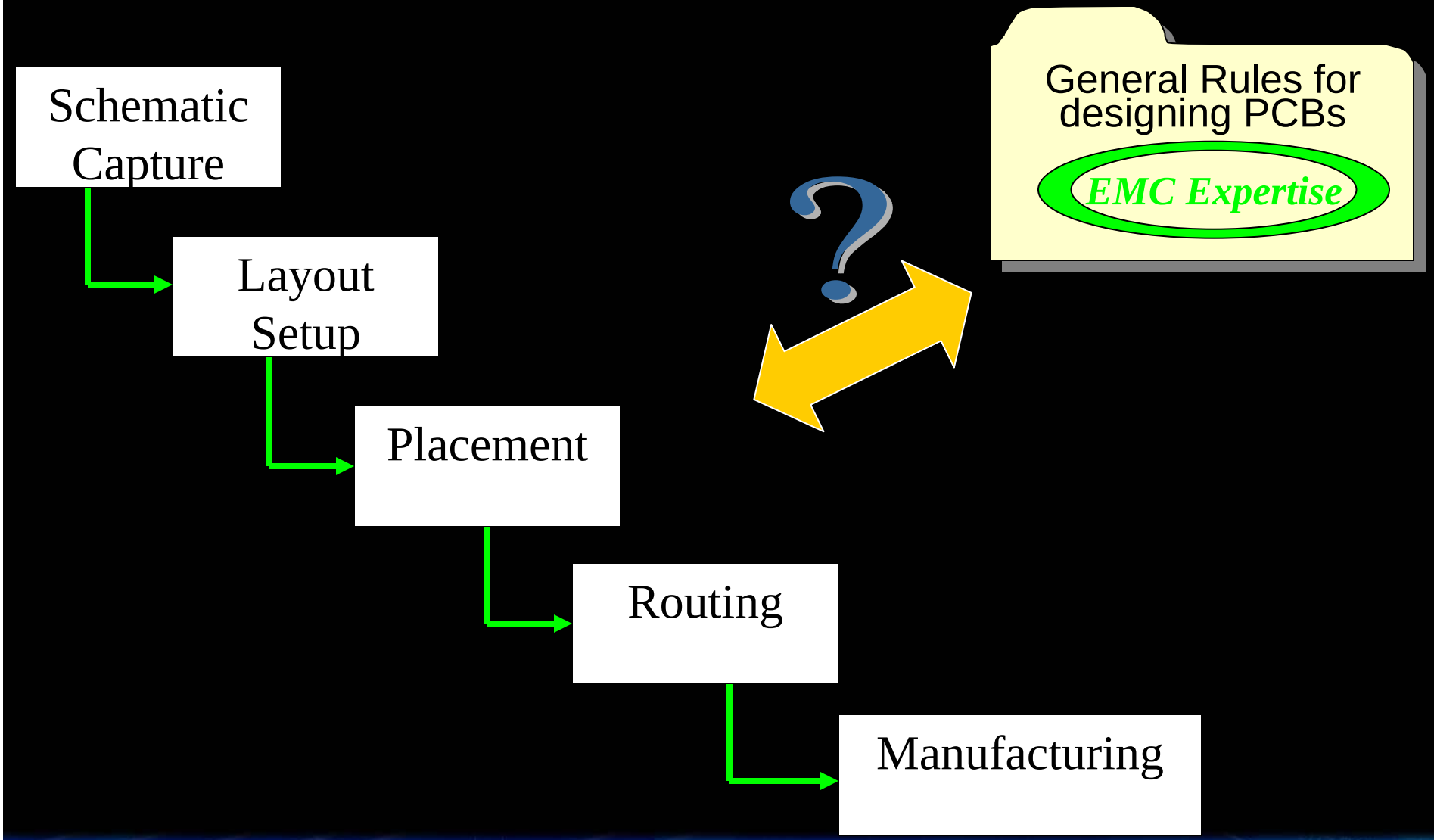


Corporate Wide Expertise



Corporate Wide Design Team usage

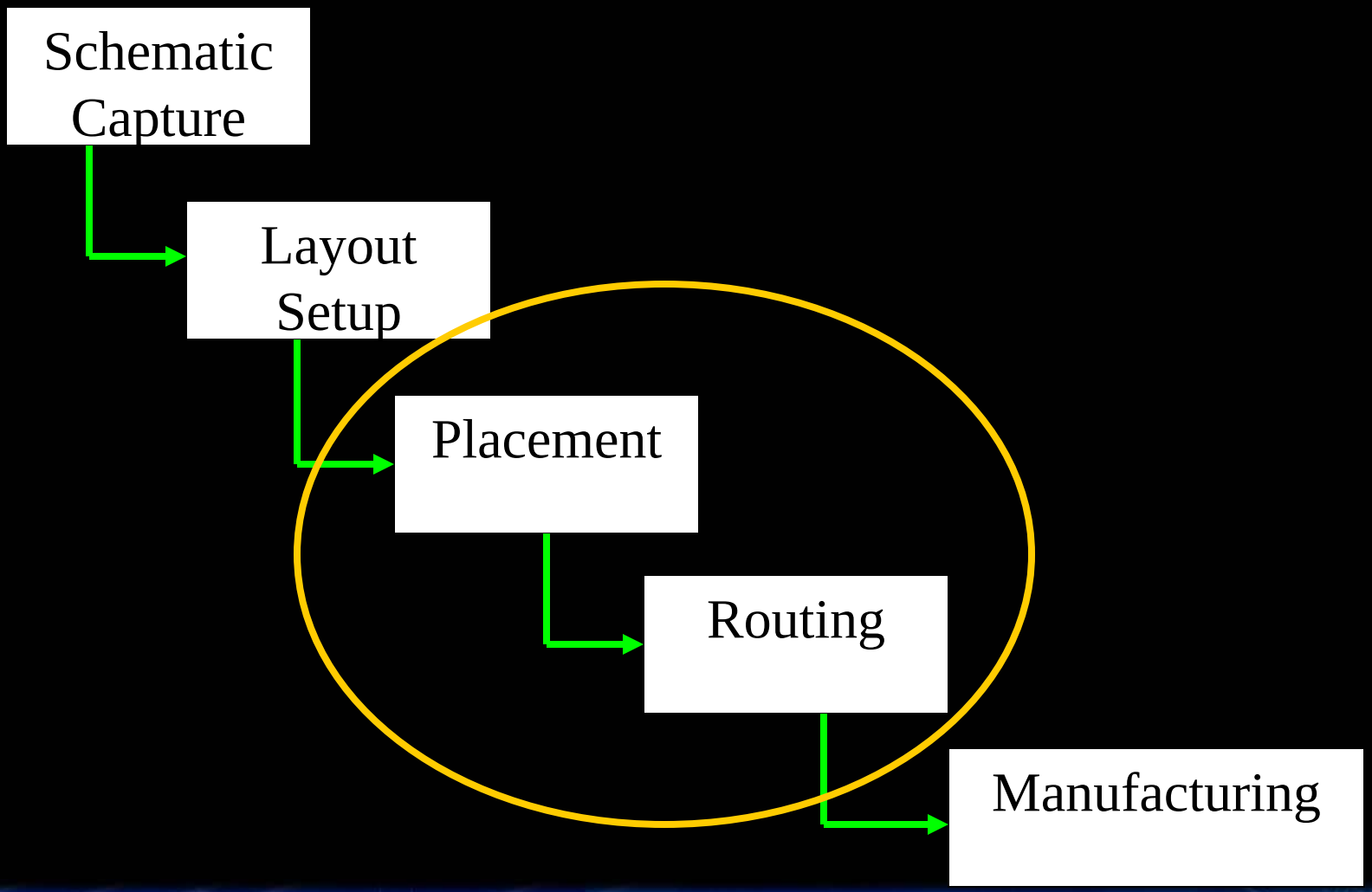
General Current Design Flow



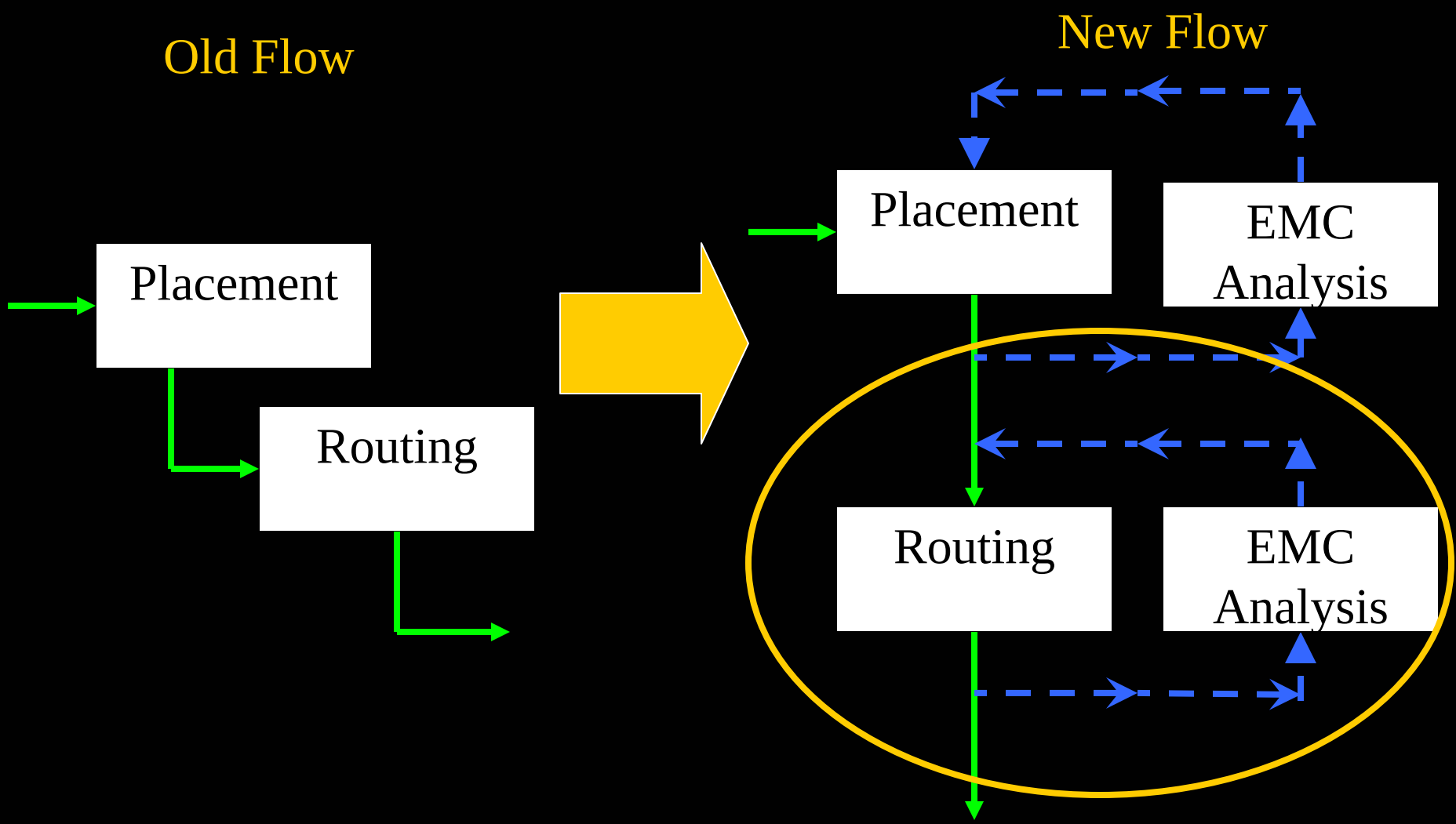
Chapter 5

How to Implement An EMI Methodology

Current Design Flow

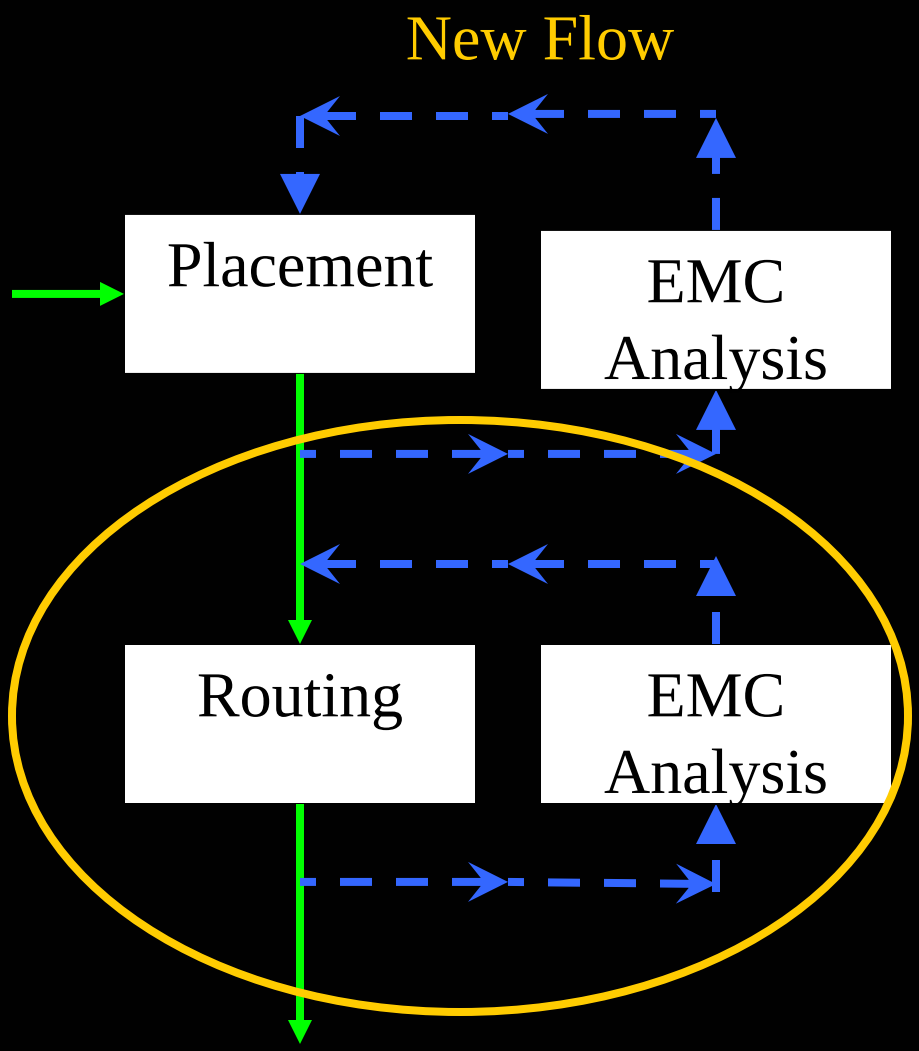


During Place and Route

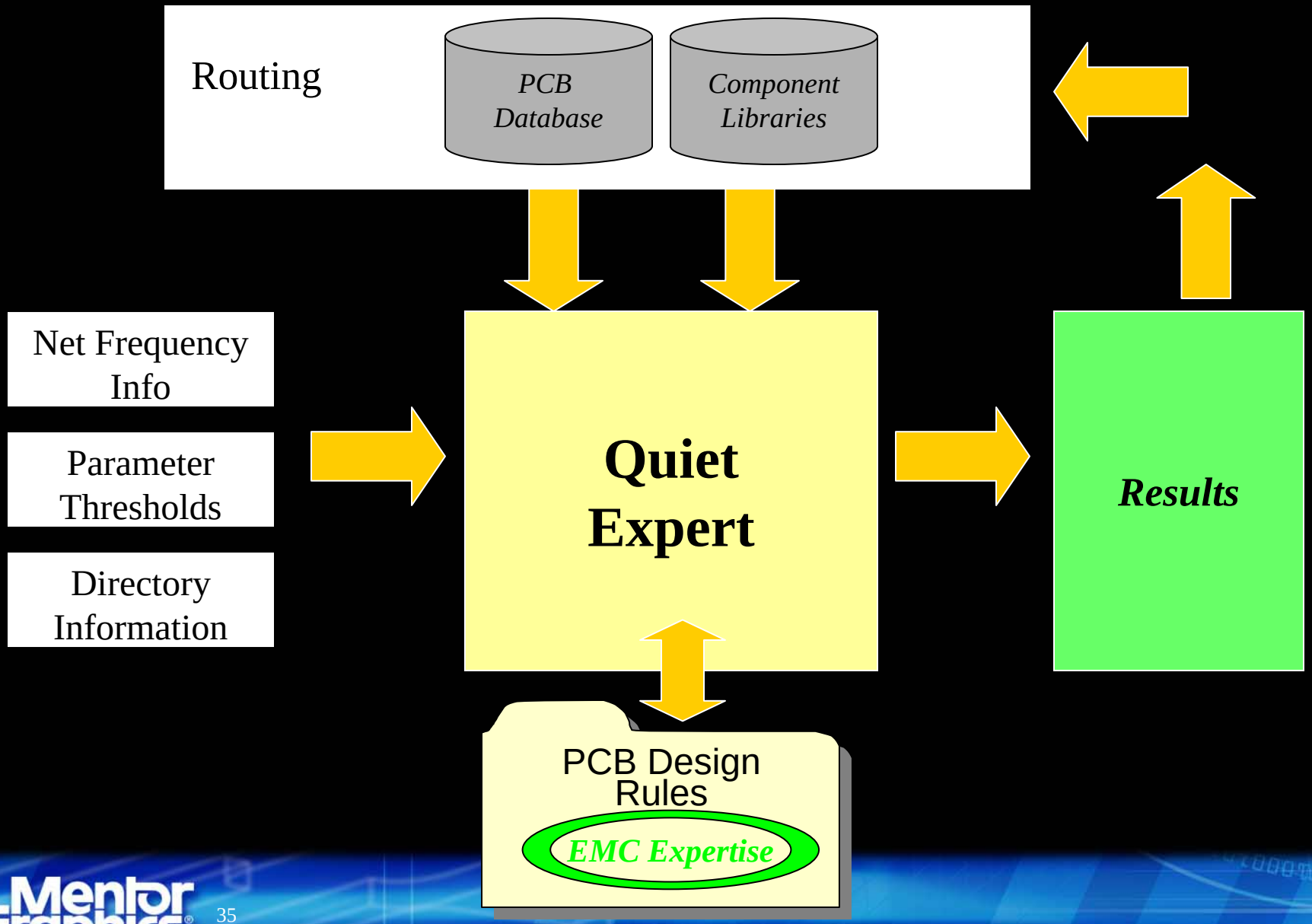


Requirements for New Analysis Loop

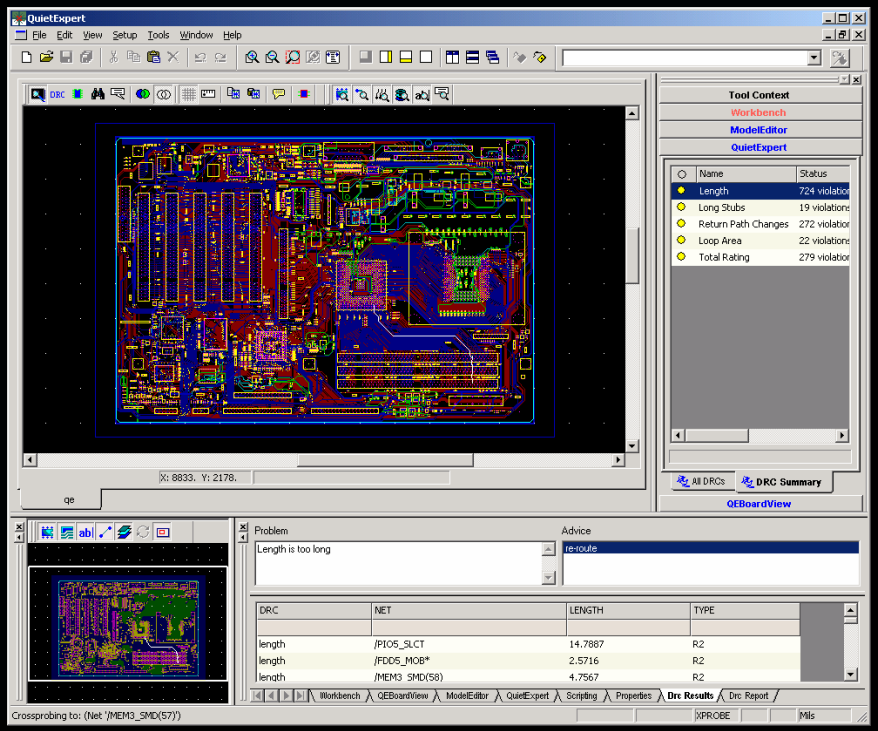
- Fast
- Easy to Use
- Integrated
- Show you exactly where the problem exists
  - Highlight net, pin, component or segment
  - Show items around the net causing the problem



EMC Analysis Tool: Quiet Expert

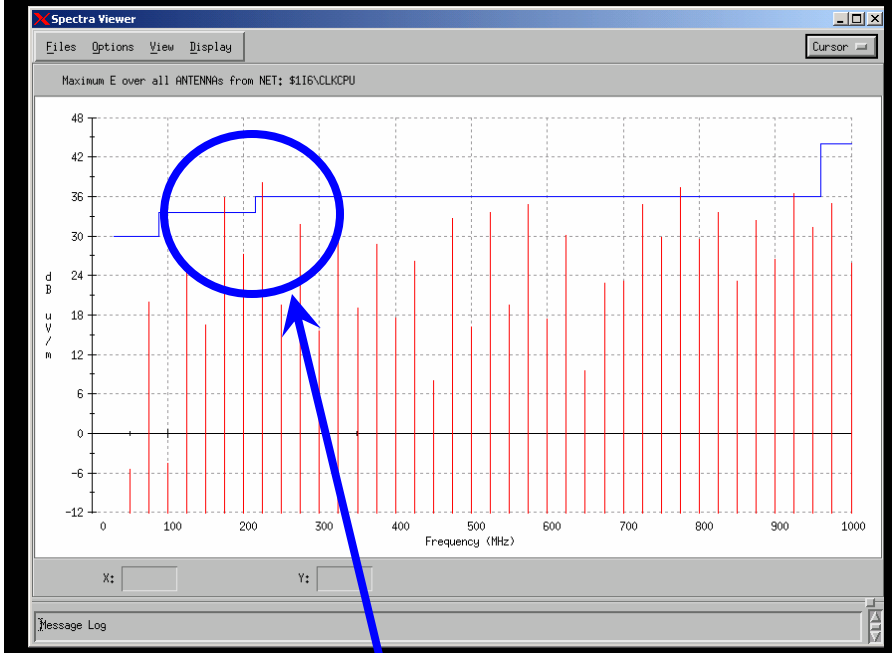


QUIET Expert
"Two tools in one"



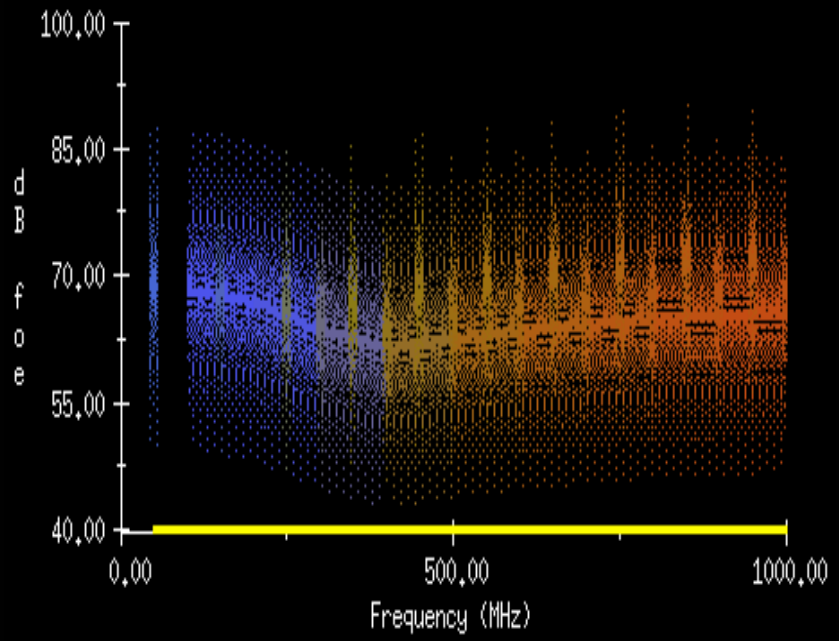
- **An EXPERT System**
  - Solves EMI problem like a Engineer not a computer
  - Makes intelligent assumptions for missing data
- **A PCB Rule Checker**
  - Physical AND Electrical checks possible
  - High-level language with access to ALL-level data.

What Results would be helpful?



"The far field measurement is showing too much EMI above 800MHz"

"EMI Compliance is missed by 2dB-uV/m at 224MHz"



DRCs make EMC simpler

- Understandable
- Show you where the problem exists
  - Highlight net, pin, component or segment
  - Show items around the net causing the problem
- Describe why it is a problem
- Give advice on how to fix the problem

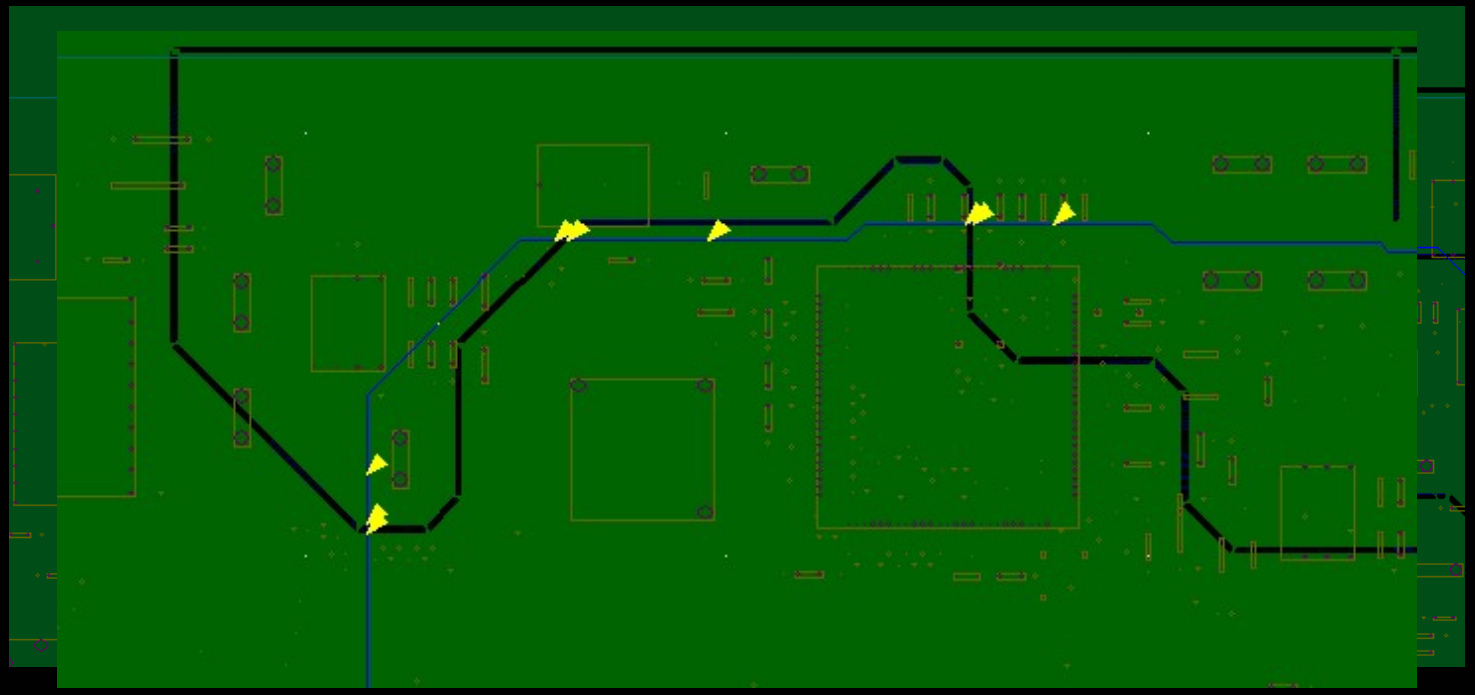
Example of Good Rules

- **Gap Crossing DRC: Do not route critical high-speed nets over gaps in ground/power plane.**
- **Decoupling DRC: Do not put the decoupling capacitor on a chip more than 5mm away from its power pin.**

Gap Crossing DRC

Signal

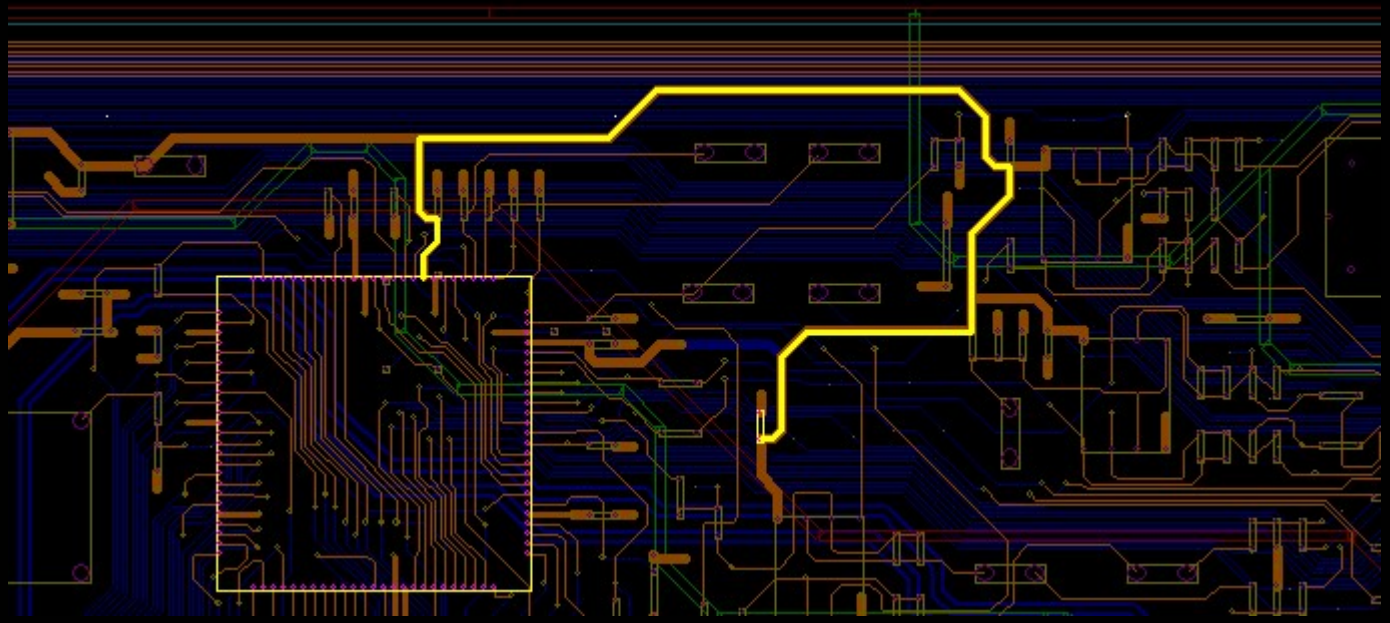
Ground



Problem: Clock net crosses more than max. allowable number of gaps(1).

Advice: Look at gap crossing areas (markers) and reroute net to reduce number of crossings

Decoupling CAP DRC



Problem: Pin to Decap Path length (12mm) more than maximum (5mm).

Advice: Reroute highlighted segment to reduce length

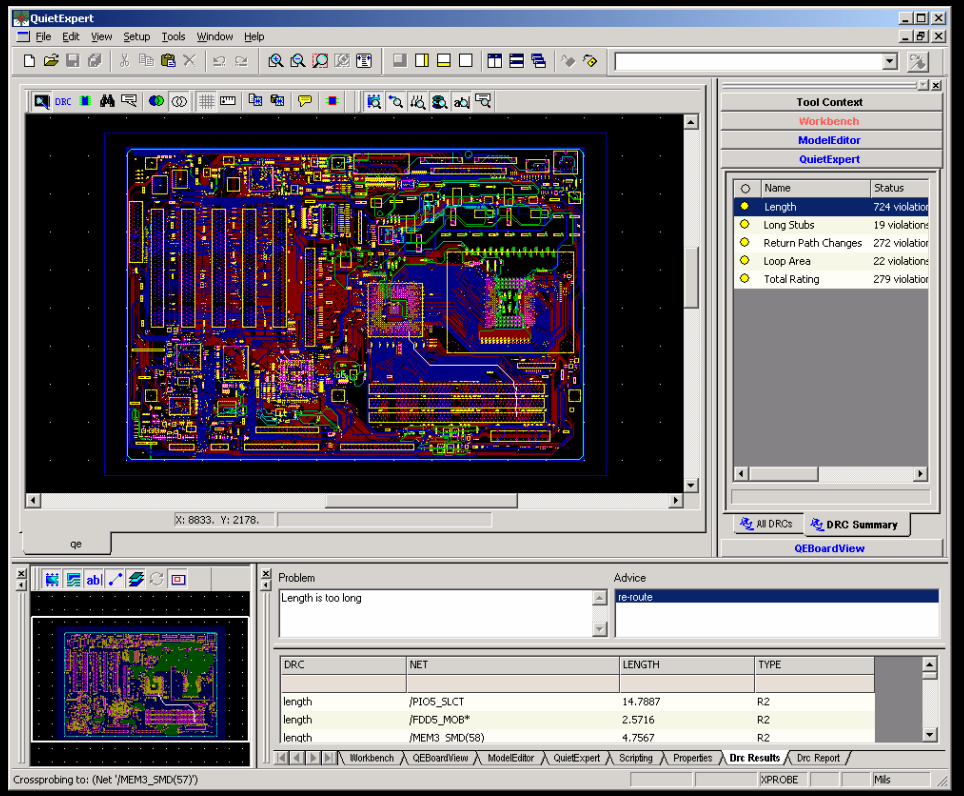
Decisions Process on Results

- Designer must be involved in some capacity in making layout changes
  - Mechanical considerations
  - Schedule considerations
  - Prioritization of rules
- Communication of results is key, especially at the end of the layout cycle
- Trade-offs are usually necessary

Quiet Expert Tool Features

Quiet Expert

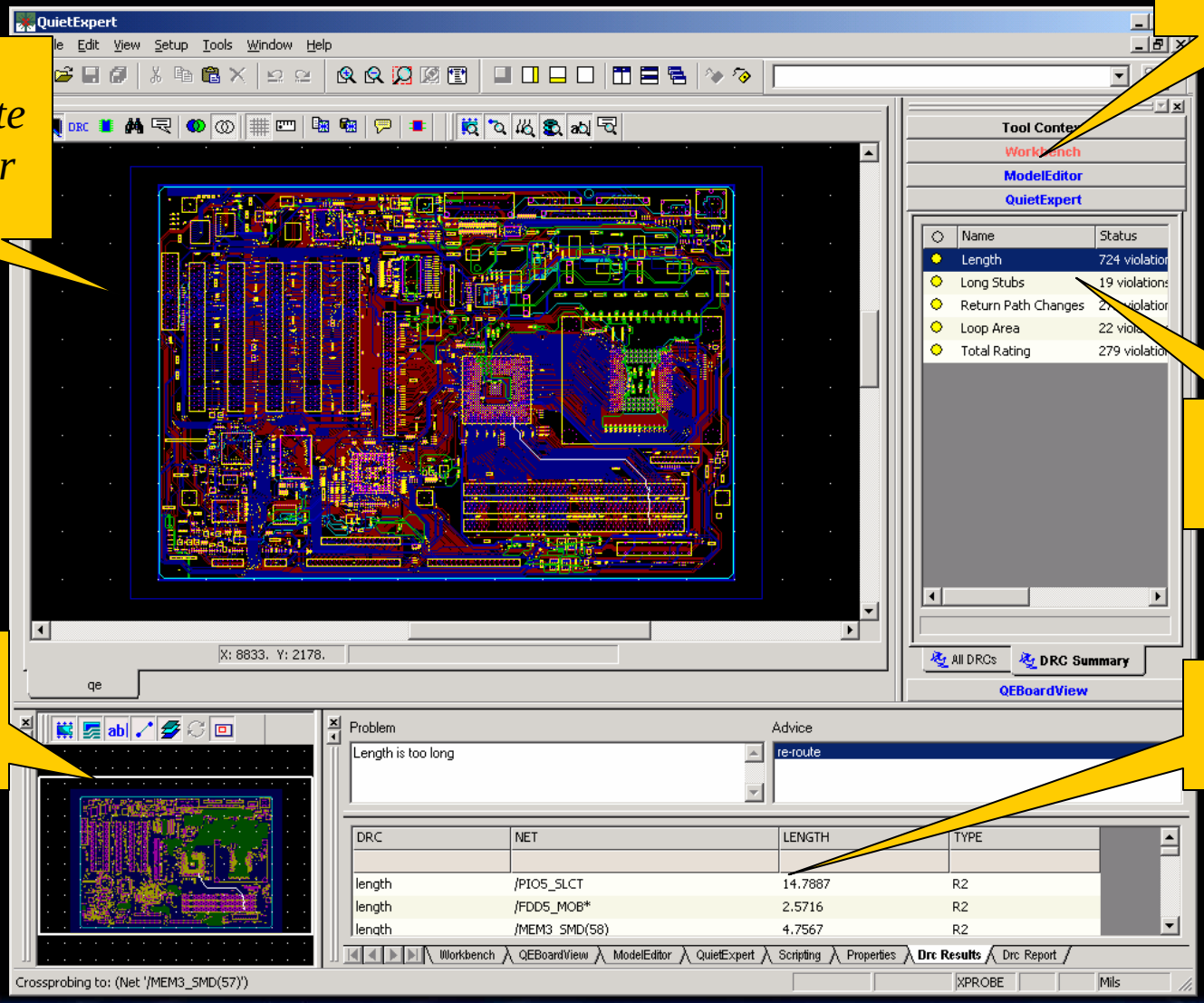
- Integrated Analysis Environment
- Quantitative information for the EMC expert
- Advice and Solutions for the non EMC expert
- Easy to use
- Incorporates IP from the University of Missouri – Rolla (UMR) EMC Consortium
- Support all major CAD flows



Enhanced GUI

Flow Control

Fast, accurate board viewer

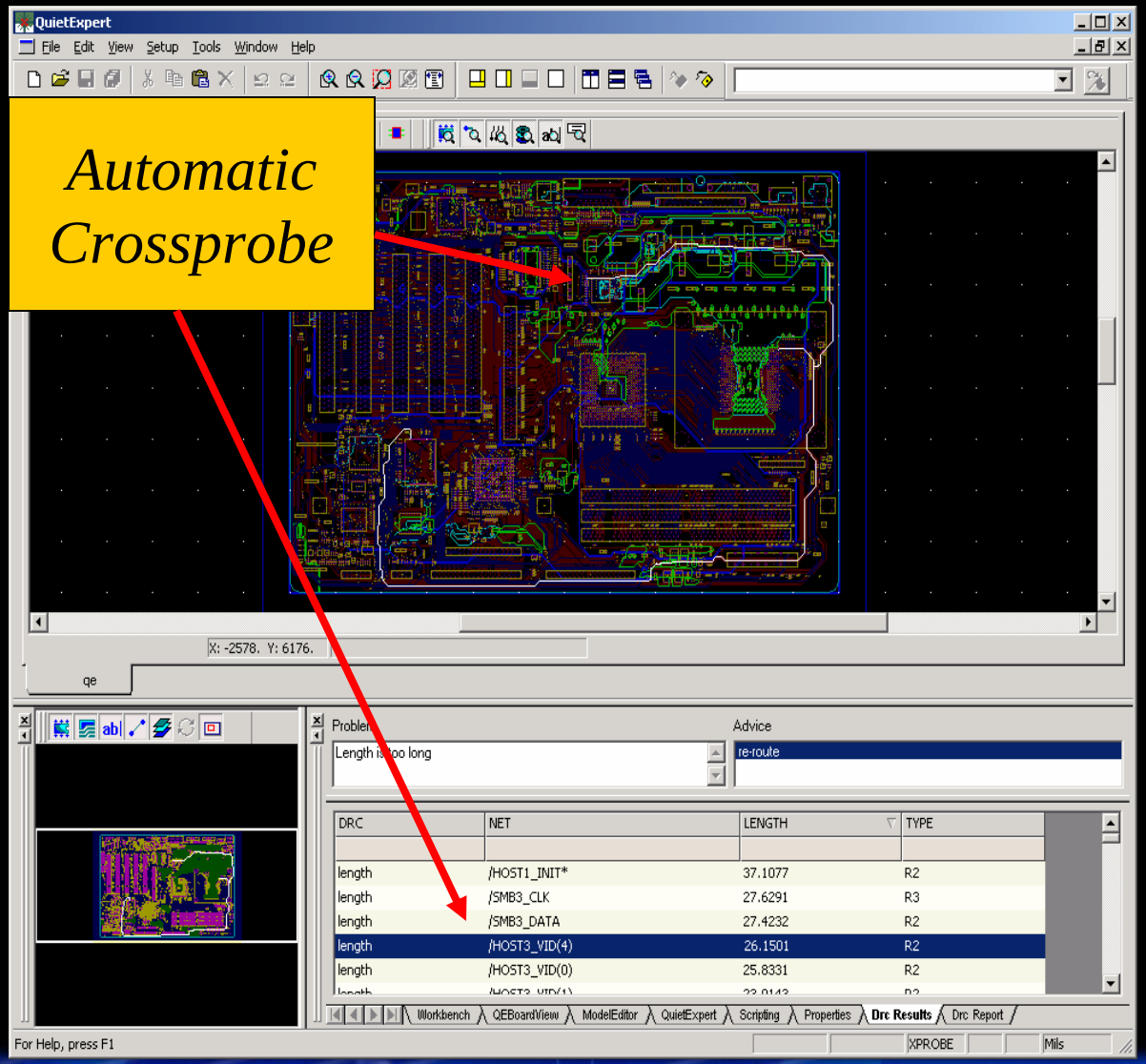


DRC List

World View window

Problems and advice

DRC Results Cross Probe

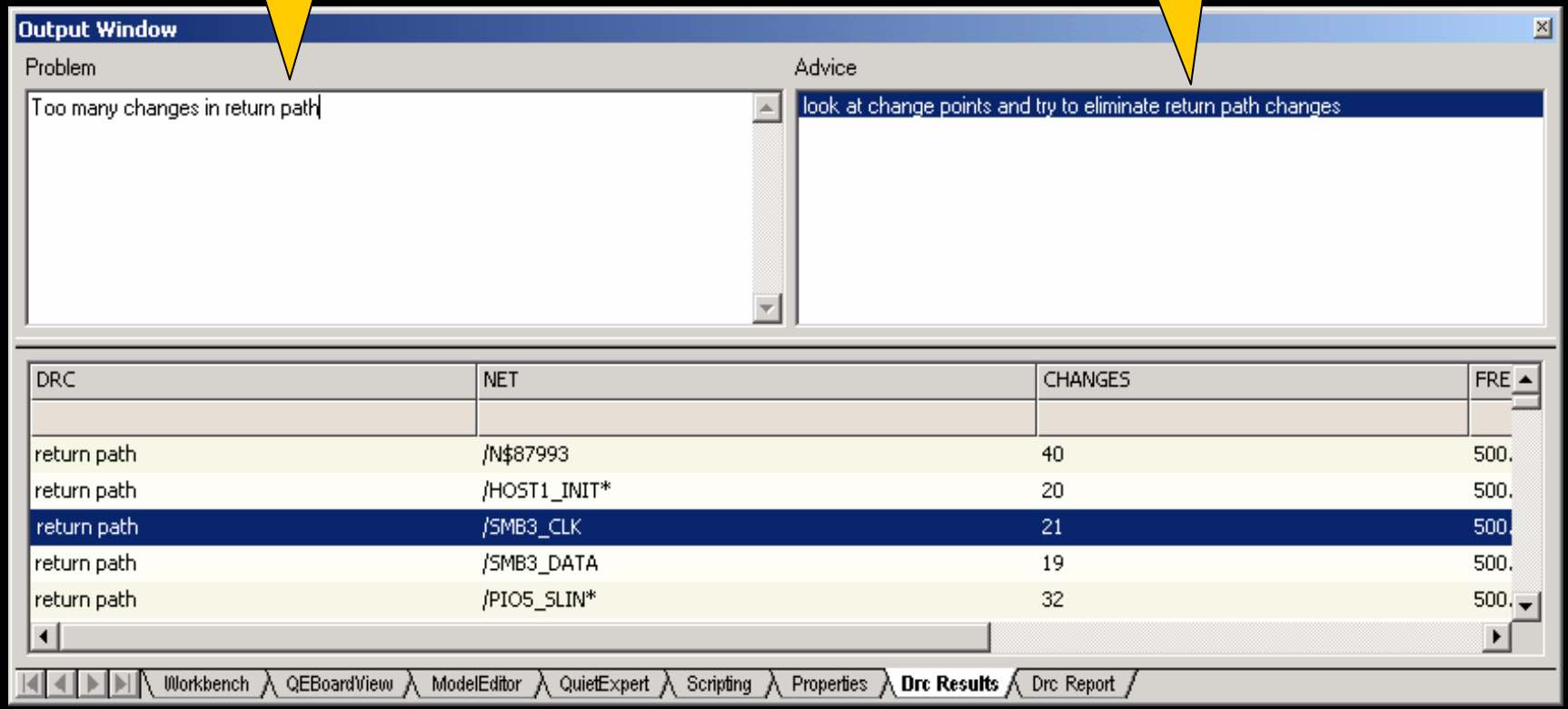


- DRC result cross probe to board viewer
- Highlighting controlled by user. Highlight by:
  - Part
  - Net
  - Segment
  - Pin, etc.
- Programming Language: TCL/TK

DRC Reporting Environment

Problem: Why is it a problem?

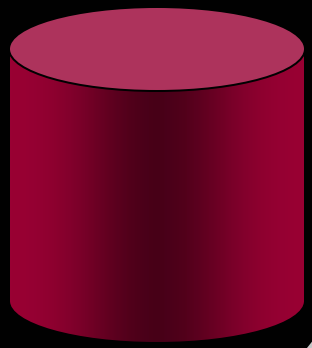
Advice: How do I Fix it?



EMC Enterprise Collaboration

Layout Team

Design Team

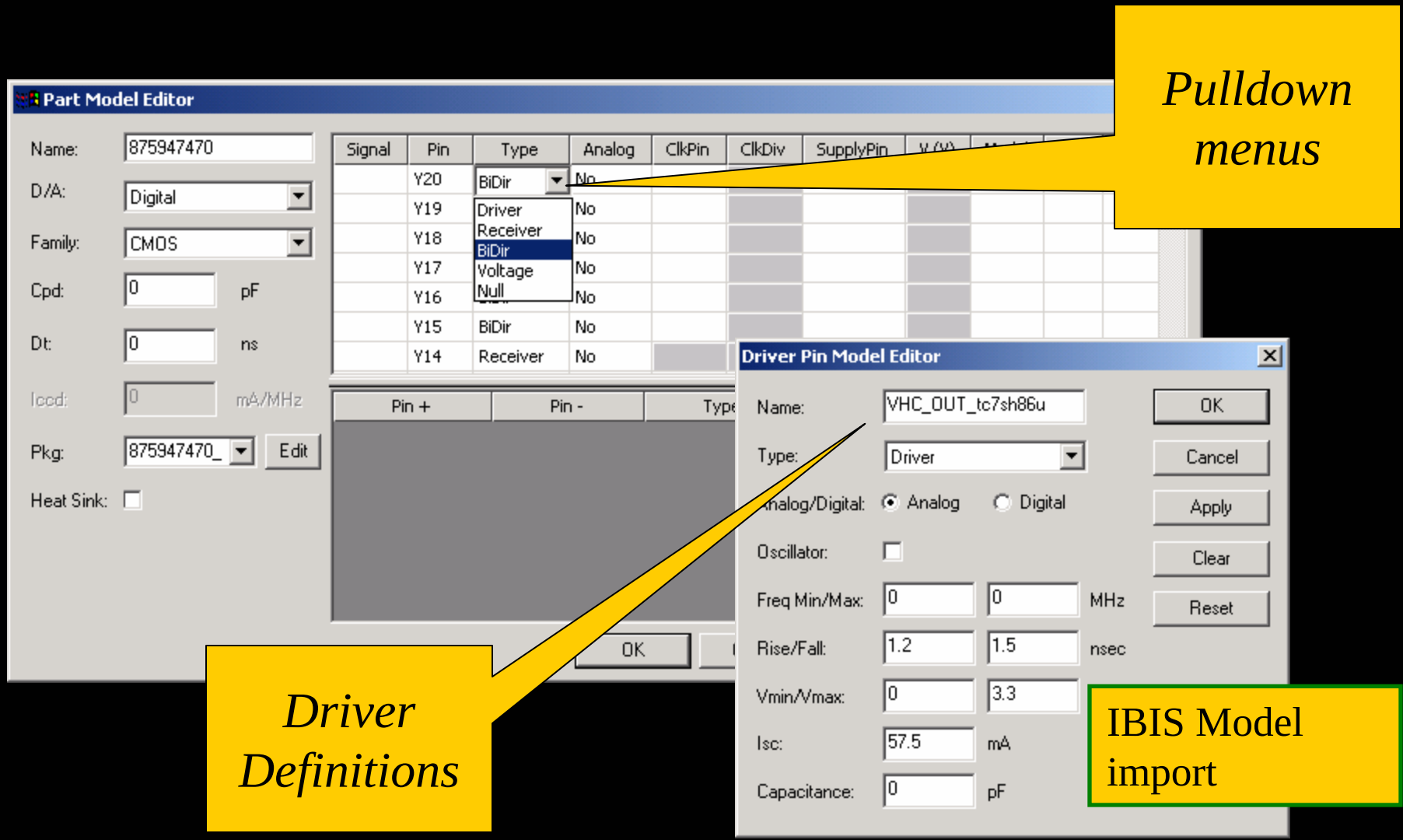


Quiet Expert Results

EMC Team

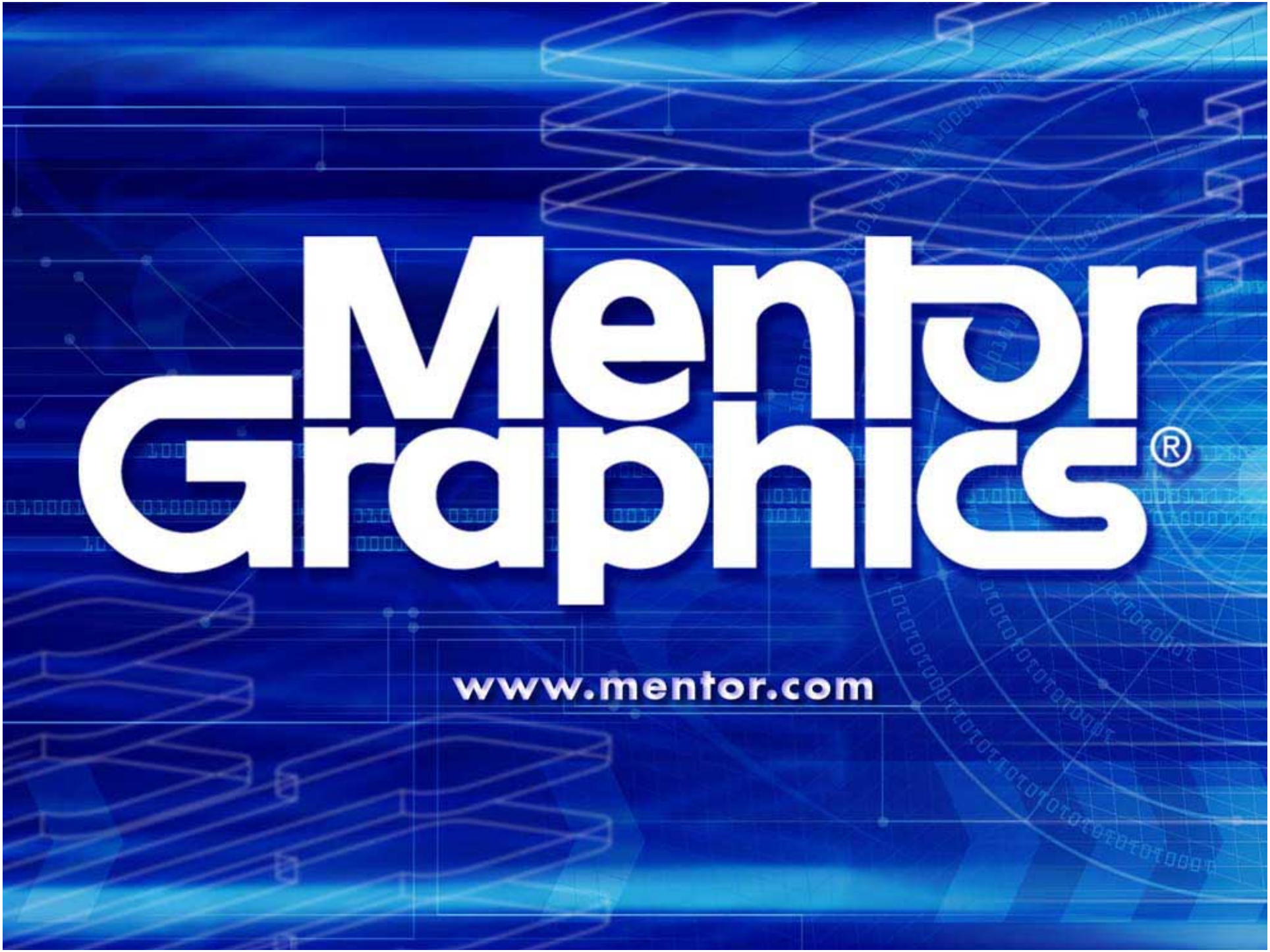
Design Collaboration ties the design team together, allowing the same information to flow through the different groups in the design flow.

Enhanced Modeling Editor



Summary

- Proper layout of PCBs significantly reduces system EMI
- Early preparation in the design cycle is the best place to fix potential EMI problems
- EMI problems non-compliance, susceptibility, system pollution and self-pollution
- Minimizing I_{dm} and Loop Area(A) reduces both Differential and Common Mode radiation
- DRCs give the quickest, most cost effective, and most understandable method to solving EMI problems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