

A Signal Integrity Simulation Case Study on Space Flight Hardware Prototypes Oct 2004

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Presentation Outline

- ✓ **Introduction – why is simulation important?**
- ✓ **Availability of advanced simulation tools**
- ✓ **Simulation setup, outputs and examples**
- ✓ **Simulation accuracy: comparing simulations to lab measurements**
- ✓ **Simulation on the James Webb Space Telescope Project**
- ✓ **Conclusion**

Introduction: Why Simulate?

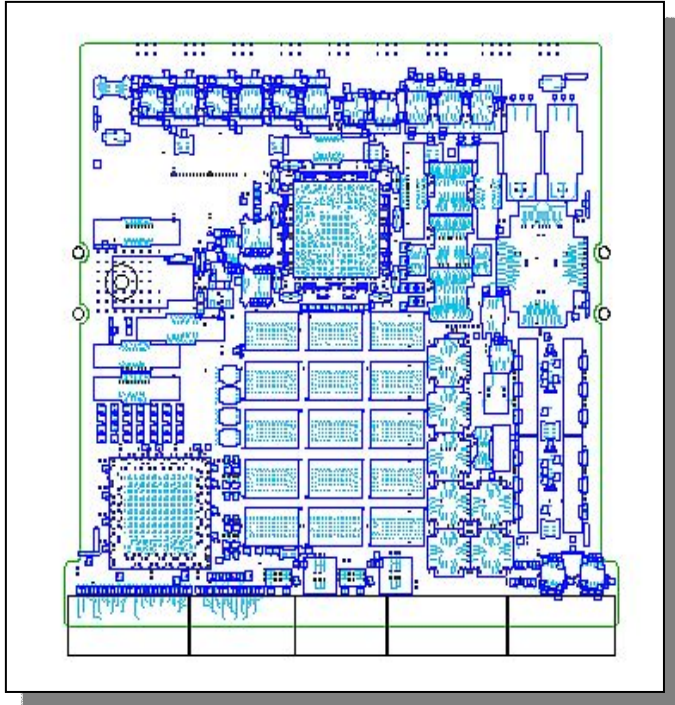
- ✓ **Signal Integrity (SI) simulation is becoming more common with the availability of quality tools that fit seamlessly with the PWB layout flow.**
- ✓ **SI simulation becomes more important with faster operational speeds and higher density requirements**
- ✓ **As device edge rates get faster it is becoming imperative to consider transmission line effects and possible signal integrity problems in the PWB design. Simulation makes it possible to do this during the layout phase without costly re-spins and difficult lab work-arounds.**
- ✓ **SI issues such as undershoot, overshoot, ringing, crosstalk, as well as power and ground integrity can be modeled and PWBs can be fabricated assuring electrical performance, which saves both cost and schedule and improves reliability and quality.**

Advanced Simulation Tools

- ✓ **In the CAD design flow, SI simulation fits into the board layout phase**
- ✓ **Both pre and post route simulation can be performed**
- ✓ **Single PCB or Multi PCB system level simulation possible.**
- ✓ **The tools that are available today are both fast and accurate**
- ✓ **Pre-route simulation is used to determine the placement of critical components, the effectiveness of the PCB stack-up structure, routing requirements for critical signal paths etc**
- ✓ **Post route simulation can be used to mitigate any potential SI or timing issues and find the solution to problems in the form of routing changes, termination schemes, optimized termination values, IO buffer selection, decoupling capacitor selection etc – all before hardware is fabricated**

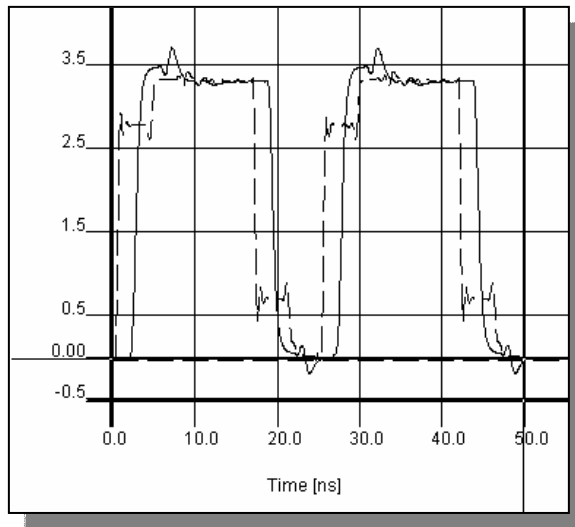
All the results in this paper were obtained using Mentor Graphics' Interconnectix Synthesis (IS) simulation tools.

Simulation Setup



- ✓ **Import CAD data into simulation tool**
- ✓ **This incorporates trace routing, via, power plane information into the simulation**
- ✓ **Define board construction, material properties**
- ✓ **Generate stimulus**
- ✓ **Classify nets: clocks, busses, control signals, static signals**
- ✓ **Define noise rules: crosstalk, over/undershoot, ringing etc**
- ✓ **Link device models to be used in simulation**

Simulation Output



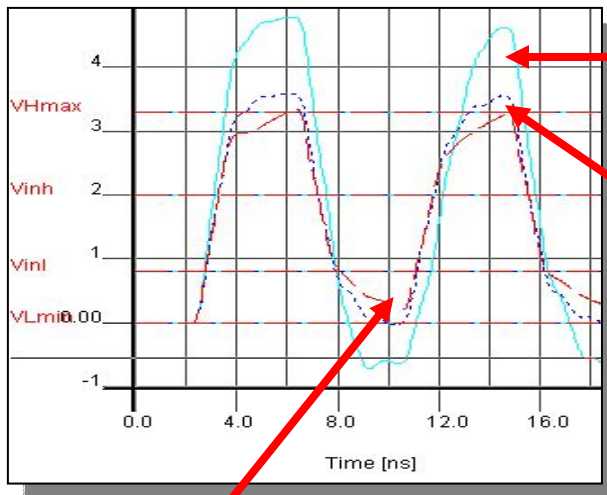
- v **Simulation provides results in various formats:**
 - Waveforms
 - Violation reports

Error Sheet				
File Edit Options Help				
	R	C	Rule Violation	Violation Data
			Undershoot	pinInst U31-B26 (Active Source U30-57) (ElectricalNet LB_MAD6) Rule: 500 mV Actual: 601.2 mV
			Undershoot	pinInst U3-A18 (Active Source U30-54) (ElectricalNet LB_MAD5) Rule: 500 mV Actual: 639 mV
			Undershoot	pinInst U31-A26 (Active Source U30-54) (ElectricalNet LB_MAD5) Rule: 500 mV Actual: 632 mV
			Undershoot	pinInst U3-B23 (Active Source U30-52) (ElectricalNet LB_MAD4) Rule: 500 mV Actual: 665.3 mV
			Undershoot	pinInst U31-A28 (Active Source U30-52) (ElectricalNet LB_MAD4) Rule: 500 mV Actual: 618.8 mV
			Undershoot	pinInst U3-B22 (Active Source U30-50) (ElectricalNet LB_MAD3) Rule: 500 mV Actual: 649.7 mV
			Undershoot	pinInst U31-B28 (Active Source U30-50) (ElectricalNet LB_MAD3) Rule: 500 mV Actual: 592 mV
			Undershoot	pinInst U3-B21 (Active Source U30-48) (ElectricalNet LB_MAD2) Rule: 500 mV Actual: 637.5 mV
			Undershoot	pinInst U31-C28 (Active Source U30-48) (ElectricalNet LB_MAD2) Rule: 500 mV Actual: 615.8 mV
			Undershoot	pinInst U3-A24 (Active Source U30-45) (ElectricalNet LB_MAD1) Rule: 500 mV Actual: 642.2 mV
			Undershoot	pinInst U31-B29 (Active Source U30-45) (ElectricalNet LB_MAD1) Rule: 500 mV Actual: 639.6 mV

Simulation Examples

v Example 1: Selecting Termination and Determining Skew

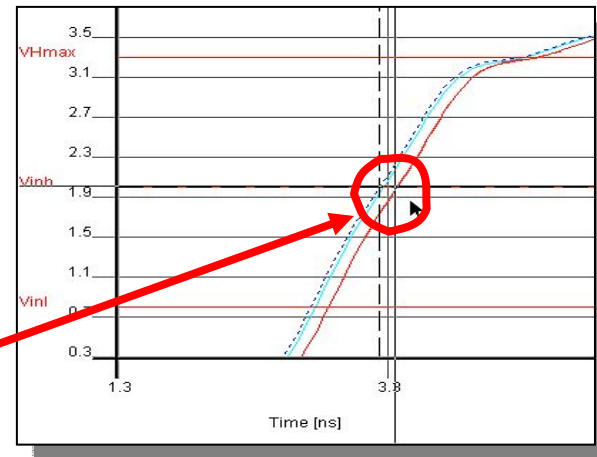
- Simulation used to select termination value and topology
- Simulation also used to determine skew between different destinations



v No termination reveals overshoot and undershoot outside of device electrical specifications

v 33 Ohm Series termination gets rid of overshoot and undershoot

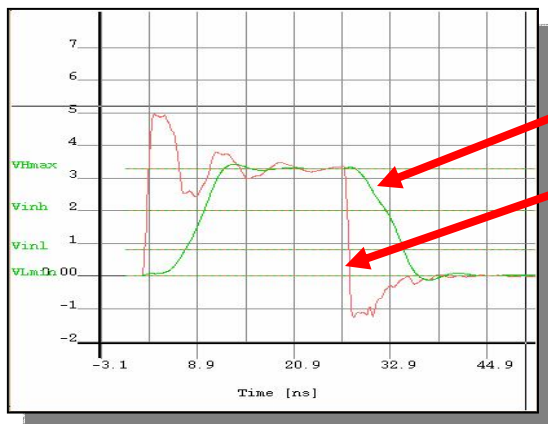
- v RC termination slows down the edge too much for the operating frequency
- v Use simulation to measure skew between various destinations to determine optimum routing, delay budget



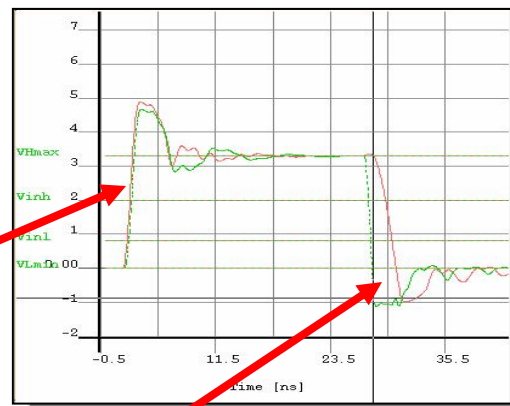
Simulation Examples

v Example 2: What-if Exploration

- Simulation used to test different device IO buffers (AX/SX, high/slow slew)
- Choose optimum IO type that meets both timing and SI requirements



- v AX slow slew driver cannot meet output timing
- v AX high slew driver violates device abs max specs

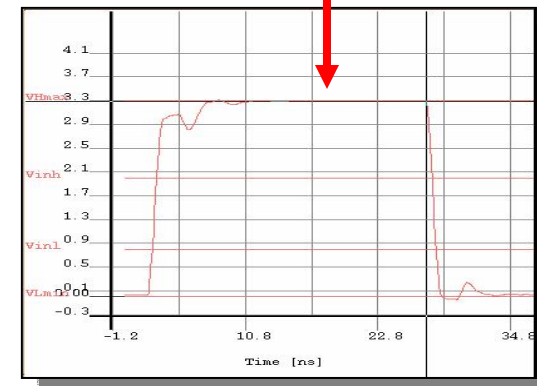


- v SX simulation shows high and slow slew have same rising edge

- v Slow slew only effects falling edge
- v SI still a problem with SX

v SI and Timing Solution:

- 45 Ohm Termination at source
- Cleans Signal, meets timing



Simulation Examples

Example 3: Running Batch Simulations

- Simulation can be used to generate summary and detailed reports of SI issues

The image displays three overlapping windows from a simulation tool. The top window is a table of violation data. The middle window shows detailed information for a specific violation (ID 3560). The bottom window is a board timing report table.

Violation Data Table:

Rule Category	Rule Violation	Violation Data
Crosstalk	Victim Net: SR_DATA0; Aggressors: BF_SPARE23; Rule: 50 mV Actual: 73.1 mV	
Crosstalk	Victim Net: SR_DATA0; Aggressors: BF_SPARE23; Rule: 50 mV Actual: 63.3 mV	
Crosstalk	Victim Net: SR_DATA0; Aggressors: BF_SPARE23; Rule: 50 mV Actual: 53.6 mV	
Crosstalk	Victim Net: SR_DATA22; Aggressors: \$19N933; Rule: 50 mV Actual: 94 mV	
Crosstalk	Victim Net: SR_DATA22; Aggressors: \$19N933; Rule: 50 mV Actual: 76.5 mV	
Crosstalk	Victim Net: SR_DATA22; Aggressors: \$19N933; Rule: 50 mV Actual: 58.2 mV	
Crosstalk	Victim Net: SR_DATA22; Aggressors: \$19N933; Rule: 50 mV Actual: 64.9 mV	

Violation Details Window:

Name: 3560 Type: Error

Noise: Error

Rule Violated: Crosstalk

Violation Data:

```

:: Crosstalk Error: (3560)
:: pinInst U47-C2
:: crosstalk method: Default
:: Victim Net: SR_BE_N6
:: Driver on victim net: U44-R28
:: Driver State: Logic0
:: Crosstalk value and its peak time from each aggressor
:: SR_ADDR_B13 U44-AA26 66.30 34.55
:: SR_ADDR_C5 U44-M26 54.20 34.55
:: SR_DATA34 U44-M34 0.10 12.45
:: Rule: 50 mV Actual: 120.3 mV
    
```

Board Timing Report Table:

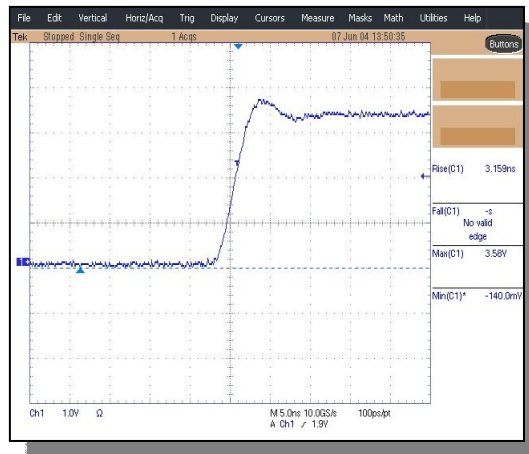
Electrical Net	Source PinInst	Load PinInst	Edge	Allowed Min Delay (ns)	Actual Min Delay (ns)	Min Alloc (ns)	Allowed Max Delay (ns)	Actual Max Delay (ns)	Max Allocator (ns)	Viol
SR_DATA0	U44-D34	U68-A7	U	2.000	0.536	0.536	8.000	4.242	4.242	yes
	U44-D34	U52-A7	U		1.233	1.233		4.284	4.284	yes
	U44-D34	U54-A7	U		1.165	1.165		4.271	4.271	yes
	U44-D34	U72-A7	U		1.011	1.011		4.255	4.255	yes
	U44-D34	U68-A7	U		0.789	0.789		4.245	4.245	yes
	U52-A7	U44-D34	U		1.485	1.485		2.266	2.266	yes
	U52-A7	U68-A7	U		1.113	1.113		2.518	2.518	yes
	U52-A7	U54-A7	U		0.474	0.474		2.971	2.971	yes
	U52-A7	U72-A7	U		0.708	0.708		2.821	2.821	yes
	U52-A7	U68-A7	U		0.929	0.929		2.648	2.648	yes
	U54-A7	U44-D34	U		1.113	1.413		2.277	2.277	yes
	U54-A7	U68-A7	U		1.086			2.463	2.463	yes
	U54-A7	U52-A7	U		0.446	0.446		2.985	2.985	yes
	U54-A7	U72-A7	U		0.732	0.732		2.749	2.749	yes

How Accurate are the Simulations?

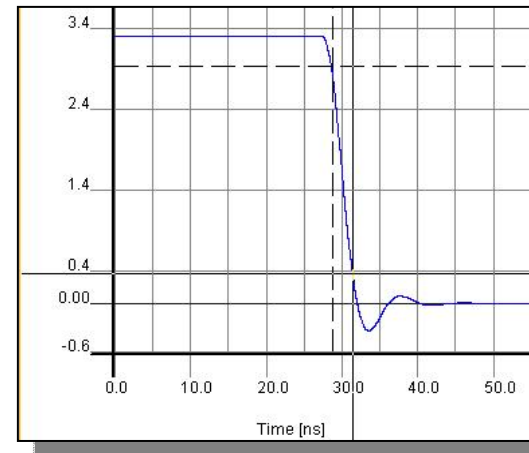
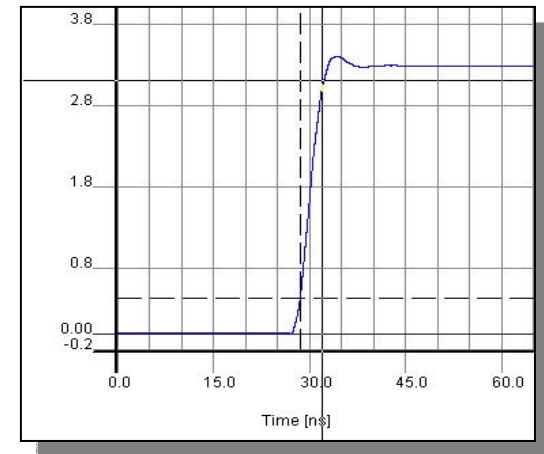
- ✓ **Simulation useful only if correlation exists to real world.**
- ✓ **Lab measurements taken on built hardware**
- ✓ **Different device drivers compared using lab measurements**
- ✓ **To date, measurements taken on Actel, Xilinx, LVDS driver devices**
- ✓ **Four examples presented, more measurements on-going**
- ✓ **Simulations found to have good correlation to actual signal**

Comparison Examples

Example 1: Xilinx Output Characteristics

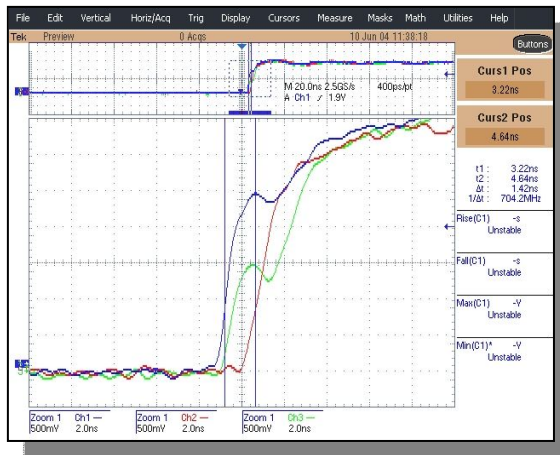


- Signal measured at receiver
- Simulation at the same point
- Rise/fall time, high/low voltage and wave shape agree closely in both simulation and lab measured results



Comparison Examples

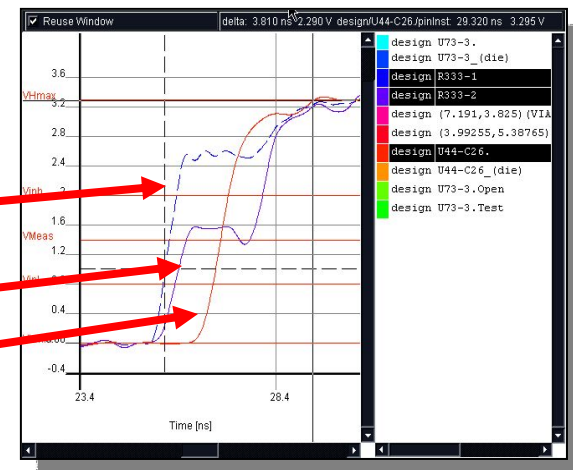
Example 2: Waveform Comparison at Three Nodes Along the Trace



- Signal measured at receiver, driver output and termination resistor pad
- The actual and simulated waveform at all 3 points agree closely
- Delay between driver output and destination input agrees
- Wave shape, voltage values agree
- Rise time at destination agree

The 3 waveforms show signal measured at:

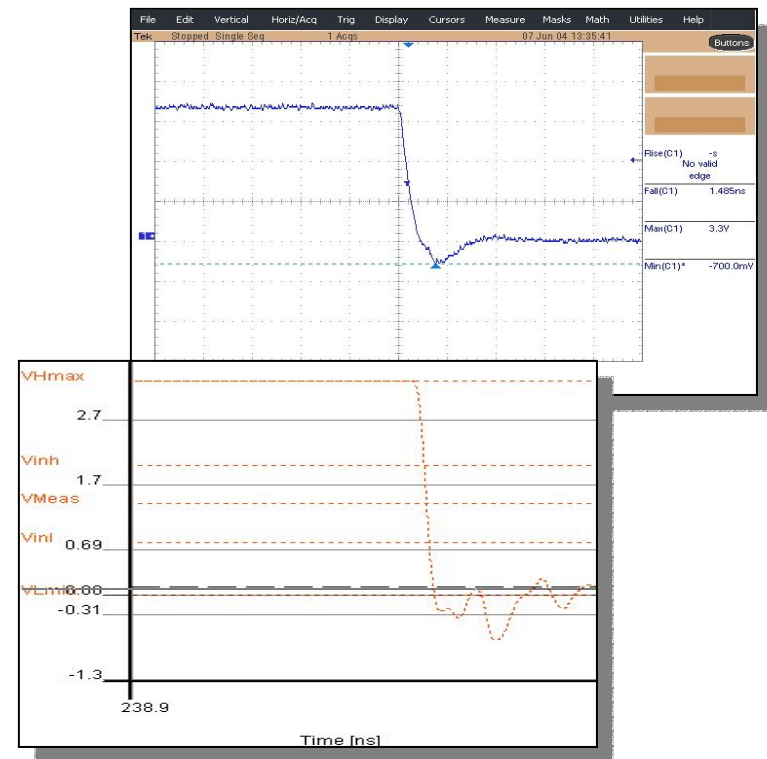
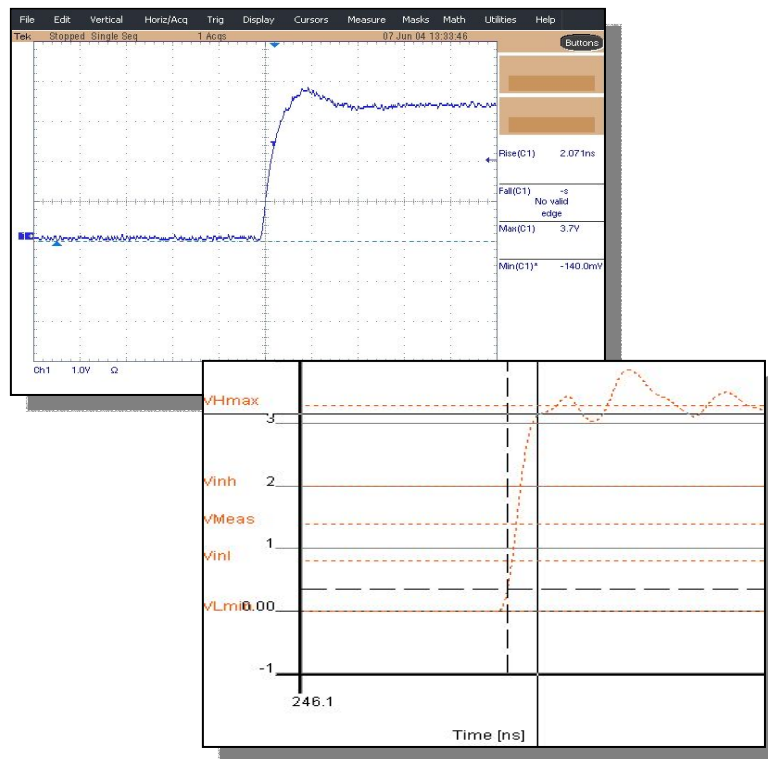
- Driver output pin (pad 1 of termination resistor)
- Pad 2 of termination resistor
- Input at destination device pin



Comparison Examples

Example 3: Actel Output Characteristics

- Voltage high/low value agree fairly closely
- Simulation shows more ringing than actual
- Rise time in lab 2.07 ns, in simulation .9 ns
- Fall time in lab 1.485 ns, in simulation .7 ns



Comparison Examples

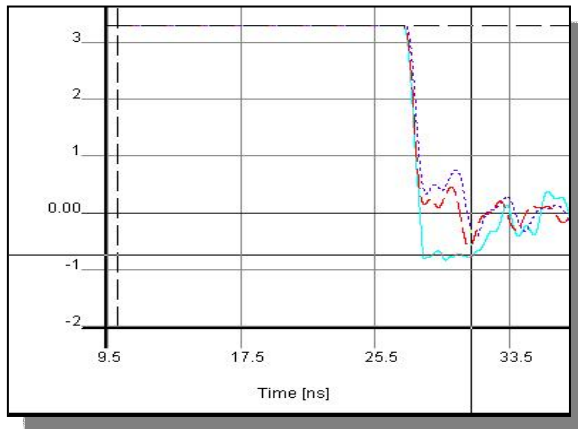
- v **Example 3 Continued: Possible reasons for mismatch**
 - Simulation assumed part directly on the board, in reality socket is installed. The socket parasitics may cause some of the variation
 - Using the min current IBIS curve, it is possible to achieve a slower rise and fall time in simulation, which is closer to the actual
 - Actel AX parts are a new device family, so the IBIS models currently available may not be representative of a typical part

- v **Future Plans to compare Actel models:**
 - Plan to re-simulate if newer AX IBIS model becomes available
 - Plan to re-take lab measurement on hardware where socket is not installed
 - Plan to do comparison measurements on hardware which has SX parts and see if similar discrepancy exists with the SX family models

Comparison Examples

v Example 4: Looking at Actel Drivers again

- Simulate 3 termination cases: 0Ohm, 45 Ohm, 56Ohm

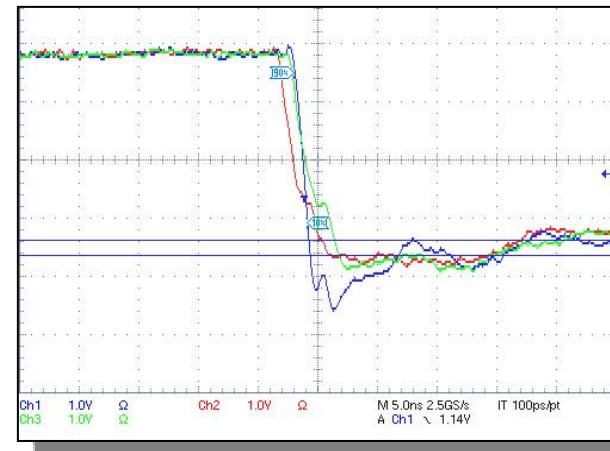


v Simulation shows:

- $\sim .9V$ undershoot with 0 Ohm
- $\sim .58V$ undershoot with 45 Ohm
- $\sim .38V$ undershoot with 56 Ohms

v Measurement shows:

- $\sim 1.1V$ undershoot with 0 Ohm
- $\sim .48V$ undershoot with 45 Ohm
- $\sim .260$ undershoot with 56 Ohm



Future of SI Simulation

- ✓ **Currently the NASA Goddard Space Flight Center is incorporating the use of simulation based SI analysis into the module design flow on the James Webb Space Telescope project.**
- ✓ **The Integrated Science Instrument Module Command and Data Handling hardware design team is using simulation tools to guarantee board performance before building hardware and will continue this methodology into the flight board designs.**
- ✓ **Currently the development units are being delivered and comparison measurements are being made in the lab with each hardware module that becomes available.**

Conclusion

- ✓ **Simply relying on traditional laboratory based SI analysis for module designs is no longer feasible due to the complexity of the circuit board designs and the changing device technologies.**
- ✓ **As designs get more complex and device families get faster, simulation tools will give design engineers an extra level of confidence in the hardware that they build and deliver**

References

- ✓ [http:// www.mentor.com/icx](http://www.mentor.com/icx)
- ✓ <http://www.actel.com>
- ✓ <http:// www.xilinx.com>

